Digital Logic Design

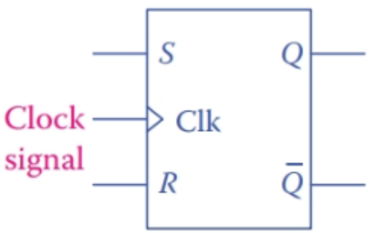
Hajar Falahati

Department of Computer Engineering
IRAN University of Science and Technology

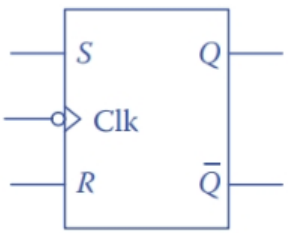
hfalahati@iust.ac.ir

Iran University of Science & Technology
IUST

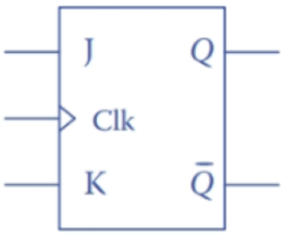
Flip Flops

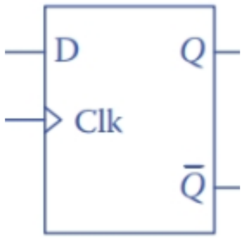


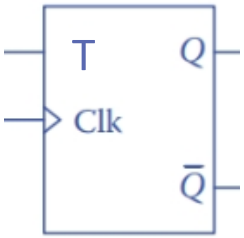
Positive edge sensitive flip-flop

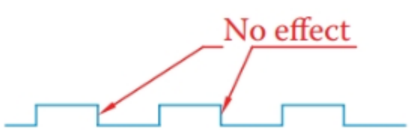


Negative edge sensitive flip-flop

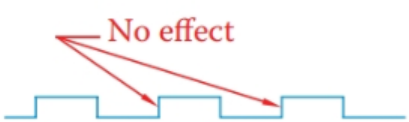








Clock signal



Clock signal

	R	S	Q	$\bar{Q}$
Hold the value	0	0	Q	$\bar{Q}$
Set the value	0	1	1	0
Reset the value	1	0	0	1
Invalid	1	1	Invalid	

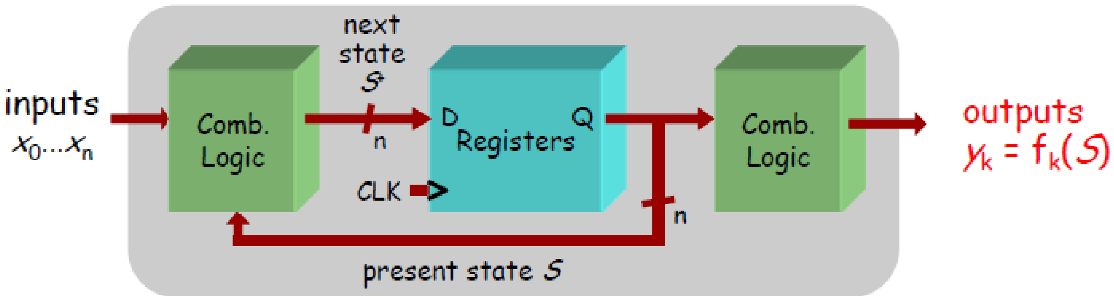
J	K	Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	Hold the value
0	1	0	1	Reset the value
1	0	1	0	Set the value
1	1	$\bar{Q}$	Q	Toggle the value

D	Q	$\bar{Q}$
0	0	1
1	1	0

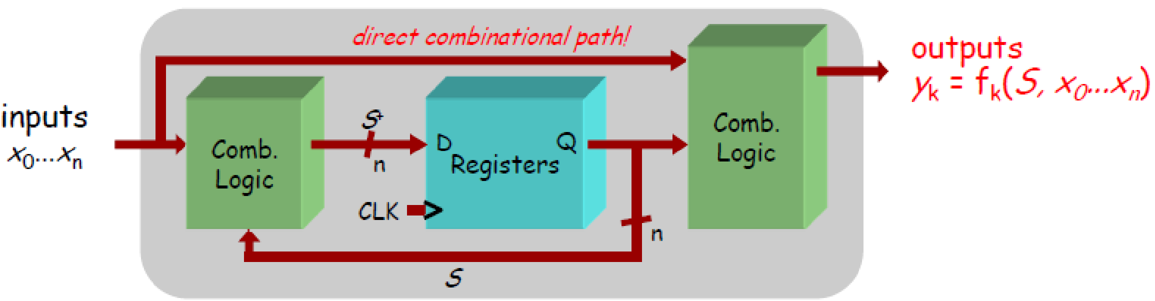
Delay FF

T	Q	$\bar{Q}$	
0	Q	$\bar{Q}$	Hold the value
1	$\bar{Q}$	Q	Toggle the value

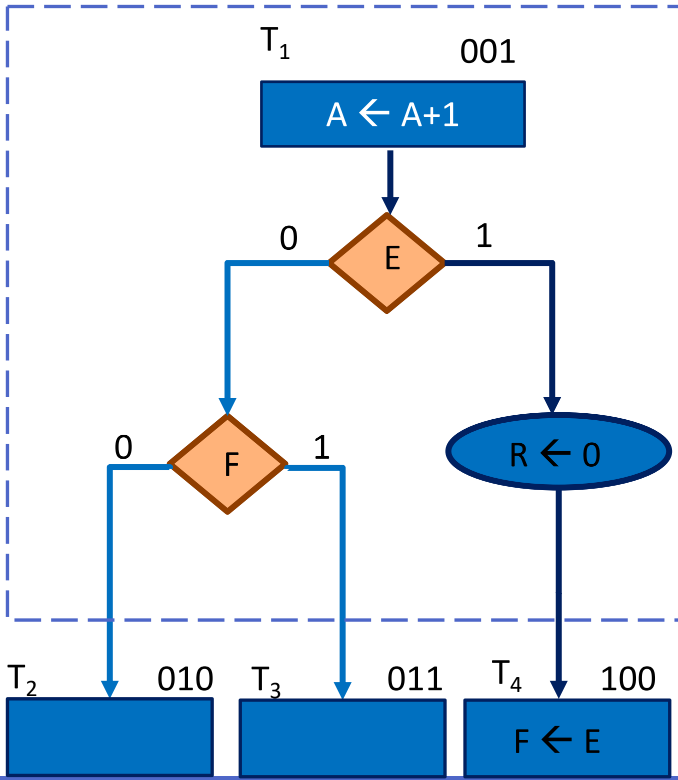
Modeling



Moore FSM



Mealy FSM



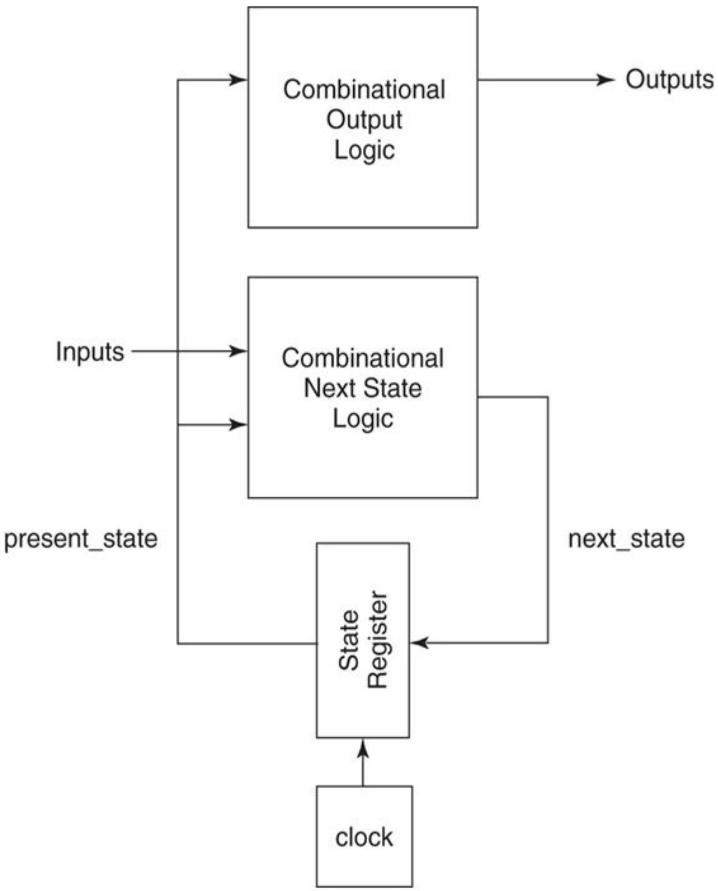
Outline

- Synthesis of Synchronous Sequential Circuits

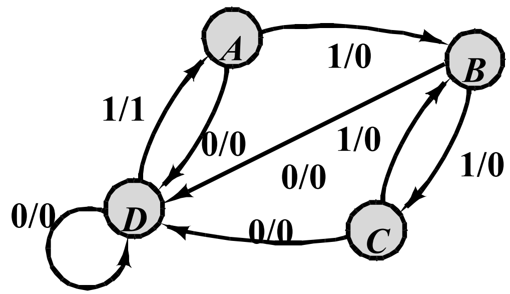
Synthesis

Synthesis

- Design a sequential circuit
- Steps
  - Specification of the required behavior
  - Create state diagram/state table
  - Determine the number of flipflops
  - Determine the type of flipflops
  - Find combinational logic to produce output
  - Find combinational logic to produce next state

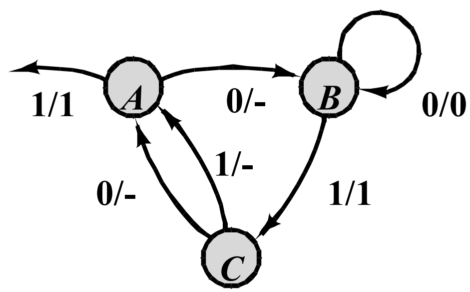


Sequential Circuit: Specification



	x = 0	x = 1
A	D/0	B/0
B	D/0	C/0
C	D/0	B/0
D	D/0	A/1

(a) Completely specified circuit

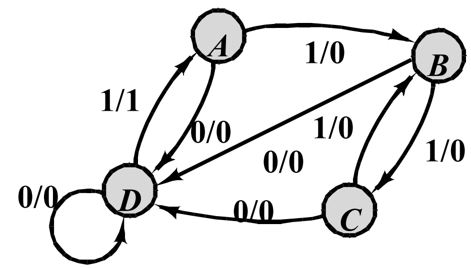


	x = 0	x = 1
A	B/-	-/1
B	B/0	C/1
C	A/-	A/-

(b) Incompletely specified circuit

Synthesis: State Assignment

- Assign codes to each state
  - **A :00**
  - **B : 01**
  - **C : 11**
  - **D: 10**



State	Q_1	Q_2	Q_3
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1

State	y_1	y_2
A	0	0
B	0	1
C	1	1
D	1	0

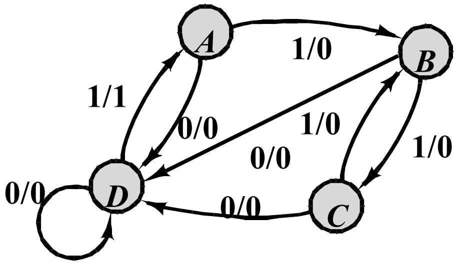
State Assignment

	$x = 0$	$x = 1$
A	$A/0$	$B/0$
B	$A/0$	$C/1$
C	$B/0$	$D/0$
D	$C/1$	$D/0$

State Table

Synthesis: Input Assignment

- Assign codes to each input
- Already done here!



State	y_1	y_2
A	0	0
B	0	1
C	1	1
D	1	0

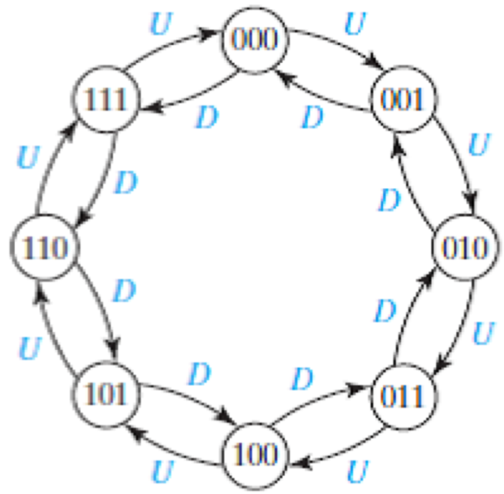
State Assignment

	$x = 0$	$x = 1$
A	$A/0$	$B/0$
B	$A/0$	$C/1$
C	$B/0$	$D/0$
D	$C/1$	$D/0$

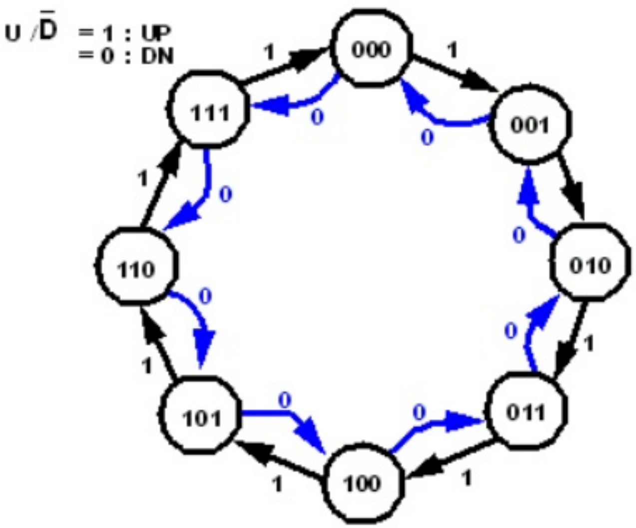
State Table

Synthesis: Input Assignment: Sample

- Assign codes to each input
  - U:1
  - D:0

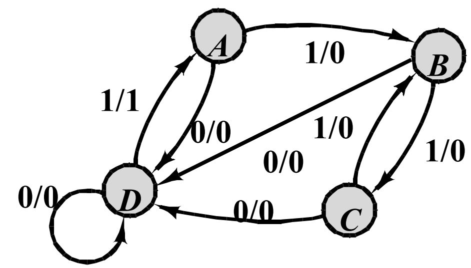


	$C^+B^+A^+$	
CBA	U	D
000	001	111
001	010	000
010	011	001
011	100	010
100	101	011
101	110	100
110	111	101
111	000	110



Synthesis: Output Assignment

- Assign codes to each output
- Already done here



State	y_1	y_2
A	0	0
B	0	1
C	1	1
D	1	0

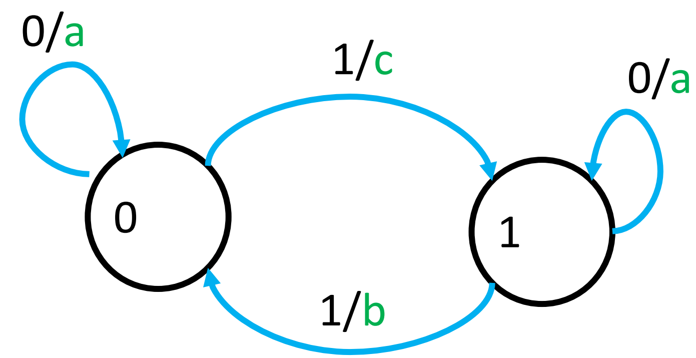
State Assignment

	x = 0	x = 1
A	$A/0$	$B/0$
B	$A/0$	$C/1$
C	$B/0$	$D/0$
D	$C/1$	$D/0$

State Table

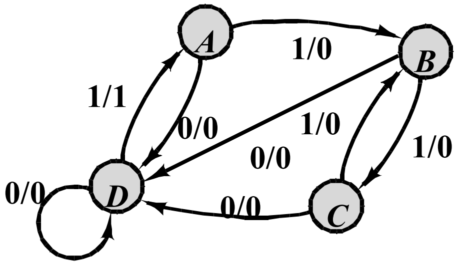
Synthesis: Input Assignment: Sample

- Assign codes to each output
  - a: 00
  - b: 01
  - c: 11



Synthesis: Transition Table

- Output: z = g (x, y)
- Excitation: Y = h (x, y)



	x = 0	x = 1
A	A/0	B/0
B	A/0	C/1
C	B/0	D/0
D	C/1	D/0

State Table

State	y_1	y_2
A	0	0
B	0	1
C	1	1
D	1	0

State Assignment

$y_1 y_2$ \ x	0	1
00	00/0	01/0
01	00/0	11/1
11	01/0	10/0
10	11/1	10/0

$Y_1 Y_2/z$

Transition Table

Synthesis: Output Simplification

- Simplifies output
  - Output: z = g (x, y)

$y_1 y_2$ \ x	0	1
00	00/0	01/0
01	00/0	11/1
11	01/0	10/0
10	11/1	10/0

$y_1 y_2$ \ x	0	1
00	0	0
01	0	1
11	0	0
10	1	0

z

$$z = x\bar{y}_1 y_2 + \bar{x} y_1 \bar{y}_2$$

Synthesis: Transistor Selection

- Determine the number and types of Flip flops
  - Excitation: Y = h (x, y)
  - Number of states
  - Two FF
  - Select D

$y_1 y_2$ \ x	0	1
00	00/0	01/0
01	00/0	11/1
11	01/0	10/0
10	11/1	10/0

$Y_1 Y_2/z$

State transitions		Required inputs
Q(t)	Q(t + e)	D(t)
0	0	0
0	1	1
1	0	0
1	1	1

(a) D flip-flop

State transitions		Required inputs	
Q(t)	Q(t + e)	S(t)	R(t)
0	0	0	*d*
0	1	1	0
1	0	0	1
1	1	*d*	0

(b) Clocked SR

State transitions		Required inputs
Q(t)	Q(t + e)	T(t)
0	0	0
0	1	1
1	0	1
1	1	0

(c) Clocked T flip-flop

State transitions		Required inputs	
Q(t)	Q(t + e)	J(t)	K(t)
0	0	0	*d*
0	1	1	d
1	0	d	1
1	1	*d*	0

(d) Clocked JK flip-flop

Synthesis: Simplification

- Find and simplifies h
  - Excitation: Y = h (x, y)
  - Select D

$y_1 y_2$ \ x	0	1
00	00/0	01/0
01	00/0	11/1
11	01/0	10/0
10	11/1	10/0

$Y_1 Y_2/z$

State transitions Q(t)	Q(t + e)	Required inputs D(t)
0	0	0
0	1	1
1	0	0
1	1	1

(a) D flip-flop

Present State		Next State X=0		Next State X=1		Y_1 X=0	Y_1 X=1
y_1	y_2	y_1	y_2	y_1	y_2	D	D
0	0	0	0	0	1	0	0
0	1	0	0	1	1	0	1
1	1	0	1	1	0	0	1
1	0	1	1	1	0	1	1

Synthesis: Simplification (cont’d)

- Find and simplifies h
  - Excitation: Y = h (x, y)
  - Select D

$y_1 y_2$ \ x	0	1
00	00/0	01/0
01	00/0	11/1
11	01/0	10/0
10	11/1	10/0

$Y_1 Y_2/z$

State transitions Q (t)	Q (t + e)	Required inputs D (t)
0	0	0
0	1	1
1	0	0
1	1	1

(a) D flip-flop

Present State		Next State X=0		Next State X=1		Y_1 X=0	Y_1 X=1
y_1	y_2	y_1	y_2	y_1	y_2	D	D
0	0	0	0	0	1	0	0
0	1	0	0	1	1	0	1
1	1	0	1	1	0	0	1
1	0	1	1	1	0	1	1

$y_1 y_2$ \ x	0	1
00	0	0
01	0	1
11	0	1
10	1	1

D_1 (= Y_1)

Synthesis: Simplification (cont'd)

- Find and simplifies h for y_2
  - Excitation: Y = h (x, y)
  - Select D

$y_1 y_2$ \ x	0	1
00	00/0	01/0
01	00/0	11/1
11	01/0	10/0
10	11/1	10/0

$Y_1 Y_2/z$

State transitions Q (t)	Q (t + e)	Required inputs D (t)
0	0	0
0	1	1
1	0	0
1	1	1

(a) D flip-flop

Present State		Next State X=0		Next State X=1		Y_2 X=0	Y_2 X=1
y_1	y_2	y_1	y_2	y_1	y_2	D	D
0	0	0	0	0	1	0	1
0	1	0	0	1	1	0	1
1	1	0	1	1	0	1	0
1	0	1	1	1	0	1	0

$y_1 y_2$ \ x	0	1
00	0	1
01	0	1
11	1	0
10	1	0

D_2 (= Y_2)

Synthesis: Simplification (cont'd)

- Find and simplifies h for y_1 and y_2
  - Excitation: Y = h (x, y)

$y_1 y_2$ \ x	0	1
00	**00/0**	**01/0**
01	**00/0**	**11/1**
11	**01/0**	**10/0**
10	**11/1**	**10/0**

$Y_1 Y_2/z$

$y_1 y_2$ \ x	0	1
00	**0**	**0**
01	**0**	**1**
11	**0**	**1**
10	**1**	**1**

D_1 (= Y_1)

$y_1 y_2$ \ x	0	1
00	**0**	**1**
01	**0**	**1**
11	**1**	**0**
10	**1**	**0**

D_2 (= Y_2)

$$D_1 = y_1 \bar{y}_2 + x y_2$$

$$D_2 = \bar{x} y_1 + x \bar{y}_1 = x \oplus y_1$$

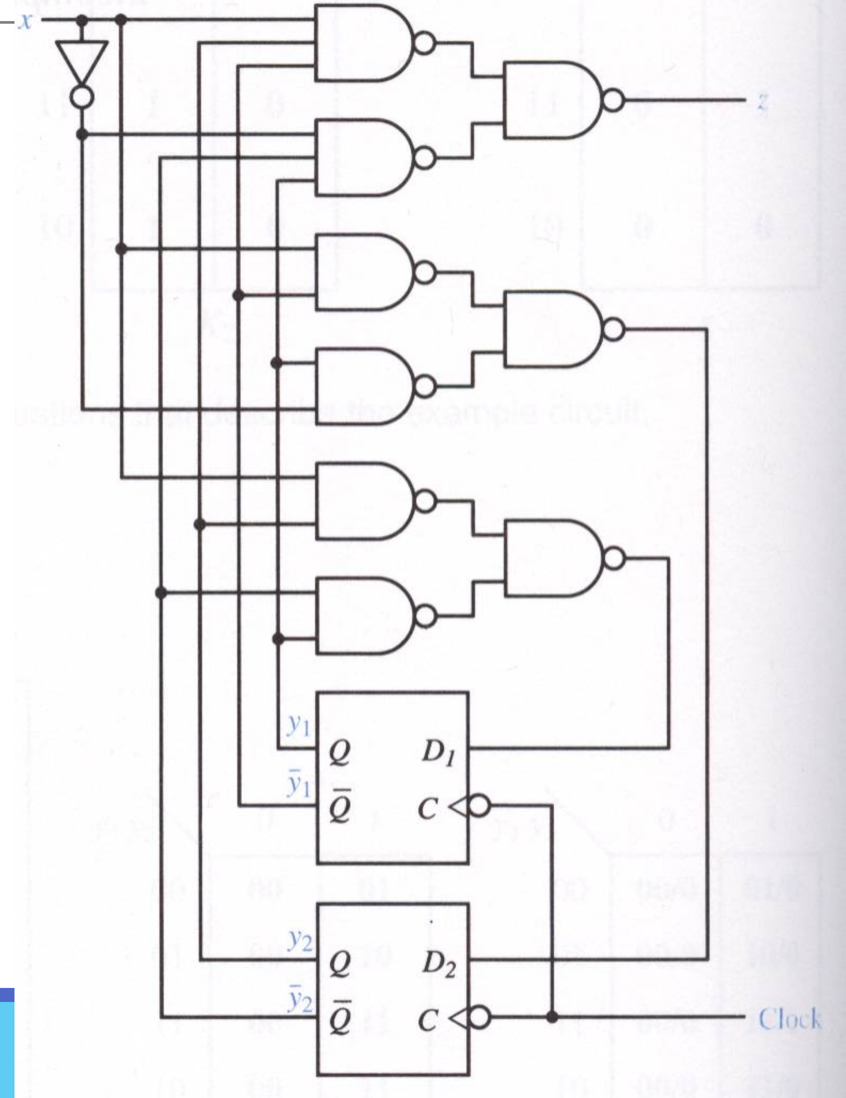
Synthesis: Realization

- Output: z = g (x, y)
- Excitation: Y = h (x, y)

$$z = x\bar{y}_1 y_2 + \bar{x} y_1 \bar{y}_2$$

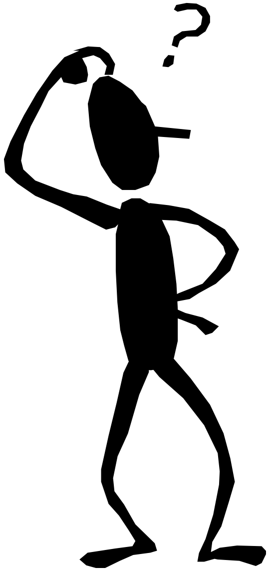
$$D_1 = y_1 \bar{y}_2 + x y_2$$

$$D_2 = \bar{x} y_1 + x \bar{y}_1 = x \oplus y_1$$



Design a Counter

- Design a synchronous bidirectional counter
  - Input $Up\ /\ \overline{Down}\ (Up)$
  - Up =1 => Counting upward
  - Up =0 => Counting downward



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Design a Counter: Step1

Present State			Next State $Up/\overline{Down}$ =1			Next State $Up/\overline{Down}$ =0			Flip Flops $Up/\overline{Down}$ =1			Flip Flops $Up/\overline{Down}$ =0		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	T_2	T_1	T_0	T_2	T_1	T_0
0	0	0	0	0	1	1	1	1			1			1
0	0	1	0	1	0	0	0	0			1			1
0	1	0	0	1	1	0	0	1			1			1
0	1	1	1	0	0	0	1	0			1			1
1	0	0	1	0	1	0	1	1			1			1
1	0	1	1	1	0	1	0	0			1			1
1	1	0	1	1	1	1	0	1			1			1
1	1	1	0	0	0	1	1	0			1			1

Design a Counter: Step1

Present State			Next State $Up/\overline{Down}$ =1			Next State $Up/\overline{Down}$ =0			Flip Flops $Up/\overline{Down}$ =1			Flip Flops $Up/\overline{Down}$ =0		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	T_2	T_1	T_0	T_2	T_1	T_0
0	0	0	0	0	1	1	1	1		0	1		1	1
0	0	1	0	1	0	0	0	0		1	1		0	1
0	1	0	0	1	1	0	0	1		0	1		1	1
0	1	1	1	0	0	0	1	0		1	1		0	1
1	0	0	1	0	1	0	1	1		0	1		1	1
1	0	1	1	1	0	1	0	0		1	1		0	1
1	1	0	1	1	1	1	0	1		0	1		1	1
1	1	1	0	0	0	1	1	0		1	1		0	1

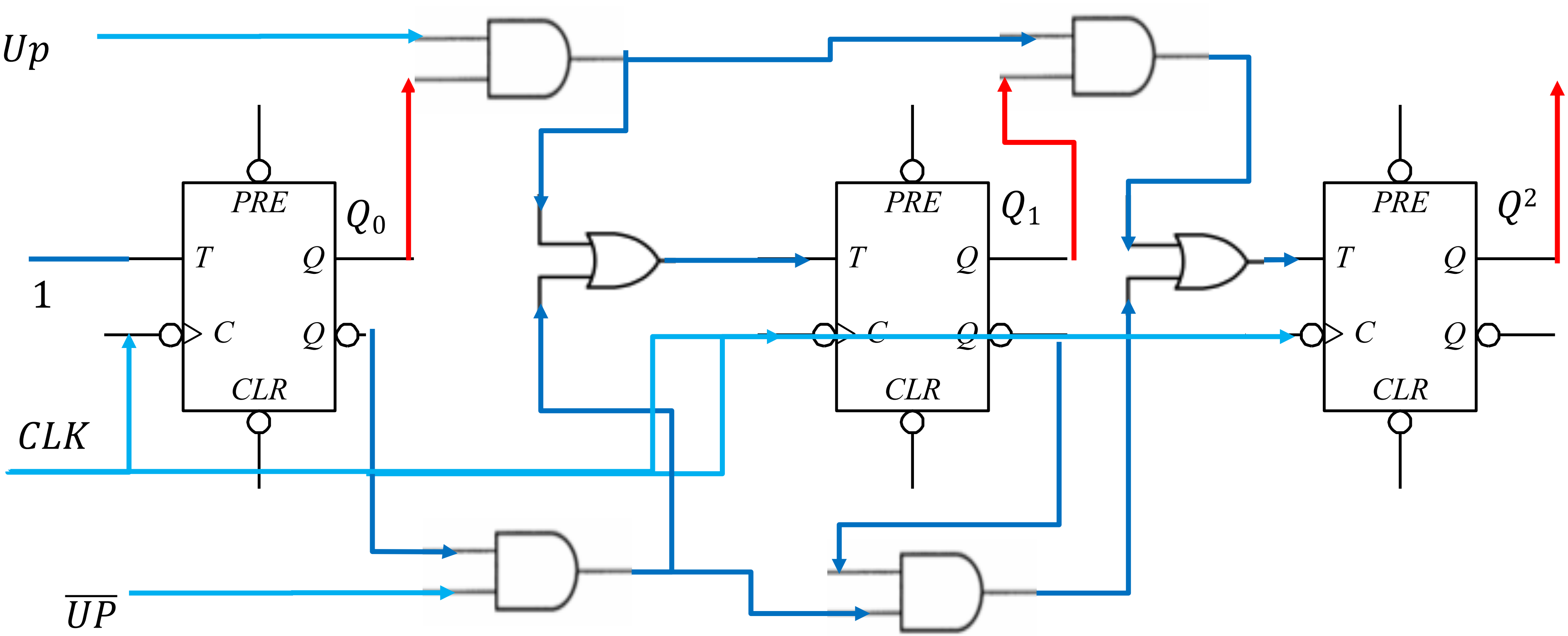
Design a Counter: Step1

Present State			Next State $Up\ /\ \overline{Down}$ =1			Next State $Up\ /\ \overline{Down}$ =0			Flip Flops $Up\ /\ \overline{Down}$ =1			Flip Flops $Up\ /\ \overline{Down}$ =0		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	T_2	T_1	T_0	T_2	T_1	T_0
0	0	0	0	0	1	1	1	1	0	0	1	1	1	1
0	0	1	0	1	0	0	0	0	0	1	1	0	0	1
0	1	0	0	1	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	1	0	1	1	1	0	0	1
1	0	0	1	0	1	0	1	1	0	0	1	1	1	1
1	0	1	1	1	0	1	0	0	0	1	1	0	0	1
1	1	0	1	1	1	1	0	1	0	0	1	0	1	1
1	1	1	0	0	0	1	1	0	1	1	1	0	0	1

$T_0 = 1$ $\quad$ $T_1 = (Q_0 Up) + \overline{Q_0} . \overline{UP}$ $\quad$ $T_2 = (Q_0 Q_1 Up) + \overline{Q_0} . \overline{Q_1} . \overline{UP}$

Design a Counter: Step1

$T_0 = 1$ $\quad T_1 = (Q_0 Up) + \overline{Q_0} . \overline{UP}$ $\quad T_2 = (Q_0 Q_1 Up) + \overline{Q_0} . \overline{Q_1} . \overline{UP}$



Thank You

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