Digital Logic Design

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Simplification

- K-map
- Q-M

Outline

- Timing Hazard
- Glitches
- Hazard-free

Hazard

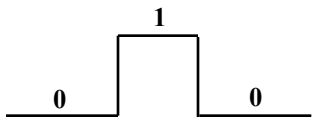
Glitch & Hazard

- Glitch
  - An unwanted pulse at the output of a combinational logic network
    - Not according to the logic
    - Caused by unequal gate propagation delays

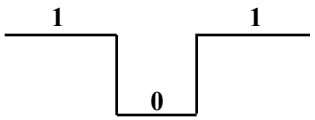
- Hazard
  - A circuit with the potential for a glitch
  - Types
    - Static
    - Dynamic

Static Hazards

- Output momentarily changes from the correct or static state
- *Static 1 hazard*
  - Output changes from 1 to 0 and back to 1
- *Static 0 hazard*
  - Output changes from 0 to 1 and back to 0



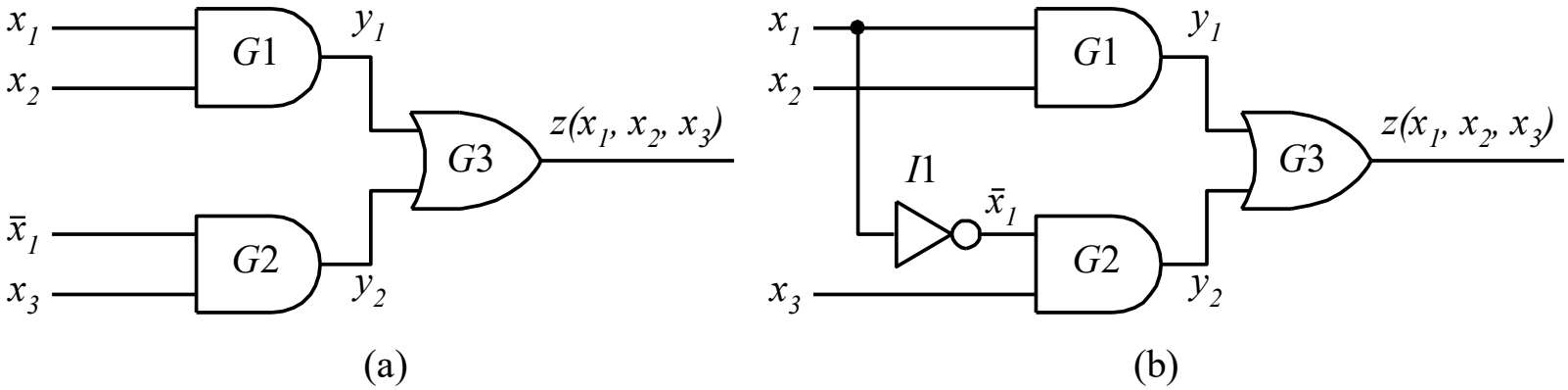
Static-0 Hazard



Static-1 Hazard

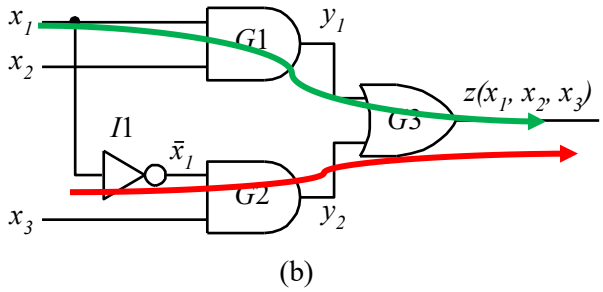
Sample1: Delay

- G1: 1 ns
- G2 = 1ns
- I1: 0.5 ns
- G3: 1 ns
- Delay?



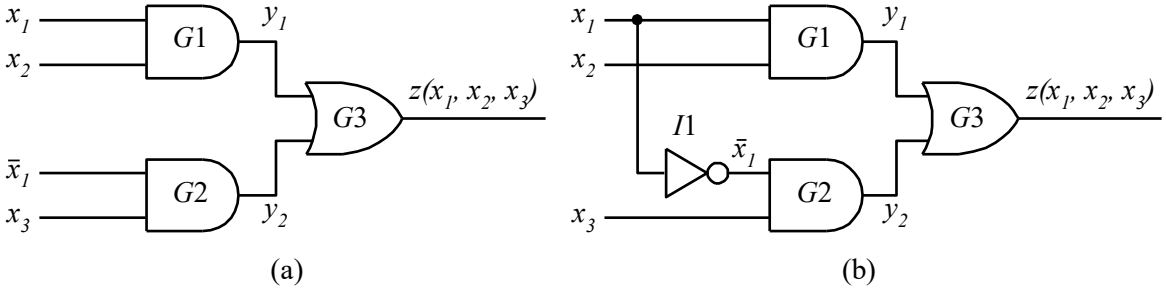
Sample1: Delay of Paths!

- Delay
  - G1: 1 ns
  - G2 = 1ns
  - I1: 0.5 ns
  - G3: 1 ns
  - Delay?
- Path 1
  - G1 , G3
  - 1 + 1 = 2 ns
- Path 2
  - I1, G2 , G3
  - 0.5+ 1 + 1 = 2.5 ns



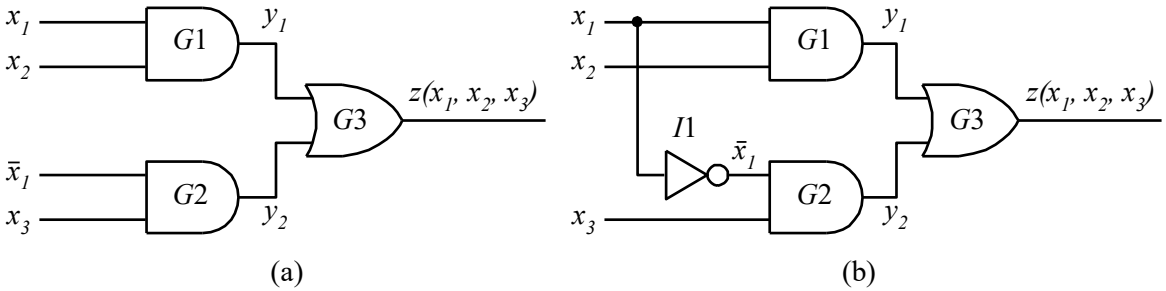
(b)

Sample1: Transient Behavior



- Transient behavior (Non zero circuit delay) :
  - Two different paths arrive at the OR gate
  - Unequal propagation delays associated with the paths
  - One path has x_1 and the other has x'_1
  - Output of the button AND gate takes longer than the output of the top AND gate

Sample1: What is the Next Value?



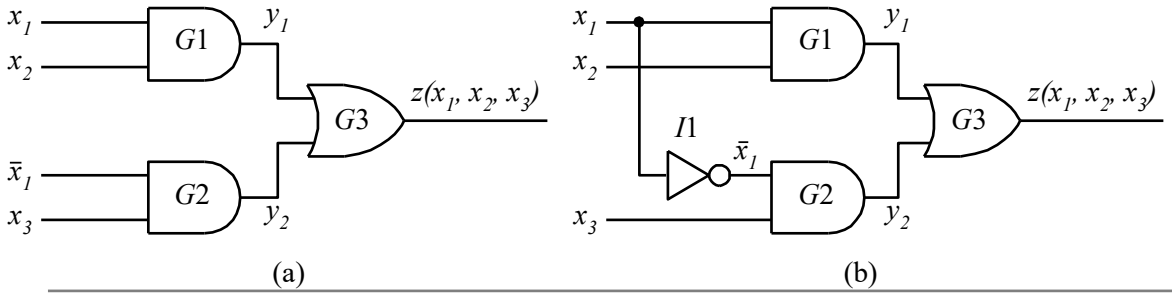
Initial values: $x_1x_2x_3 = 000$, $Z = 0$

Next values: $x_1x_2x_3 = 111$

$y_1 = x_1 x_2 = 1$

$y_2 = x'_1 x_3 = 1$

$z = y_1 + y_2 = 1$

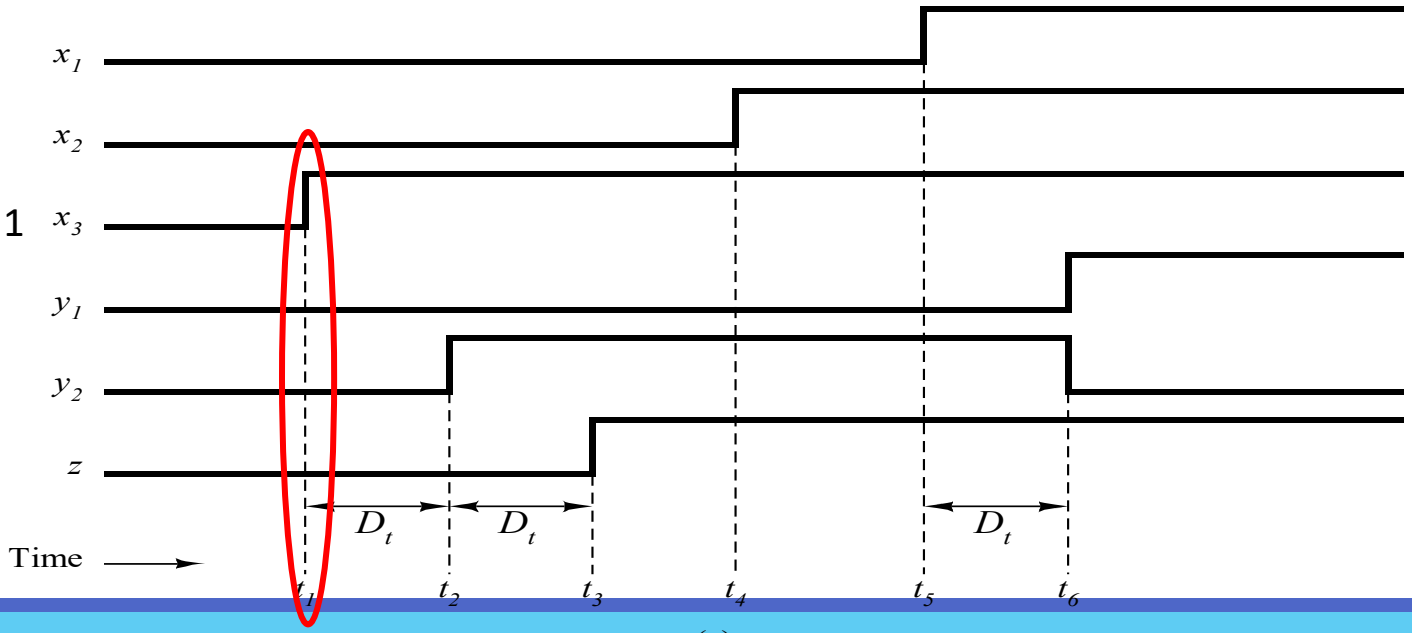


Initial values: $x_1x_2x_3 = 000$, $z = 0$

Input change t_1: x_3 0 -> 1

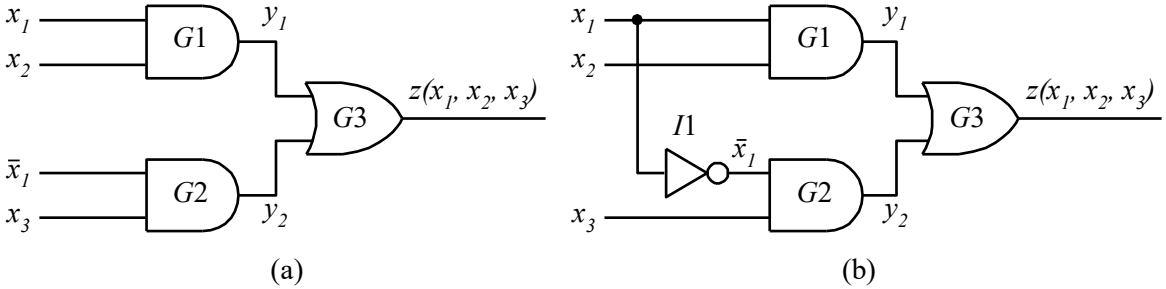
$y_2 = x'_1 x_3 = 0$

$z = y_1 + y_2 = 0$



(c)

Sample1: Timing Analysis (cont'd)

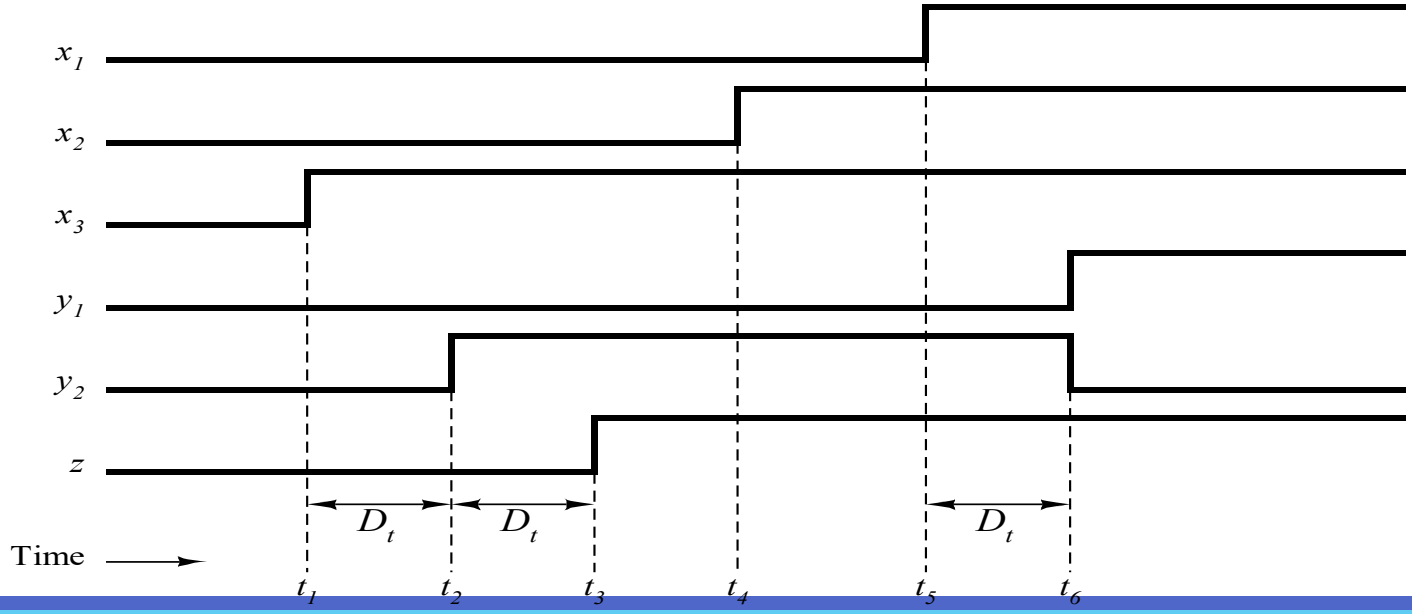


Initial values: $x_1x_2x_3 = 000$, $z = 0$

Input change t_4: x_2 0 -> 1

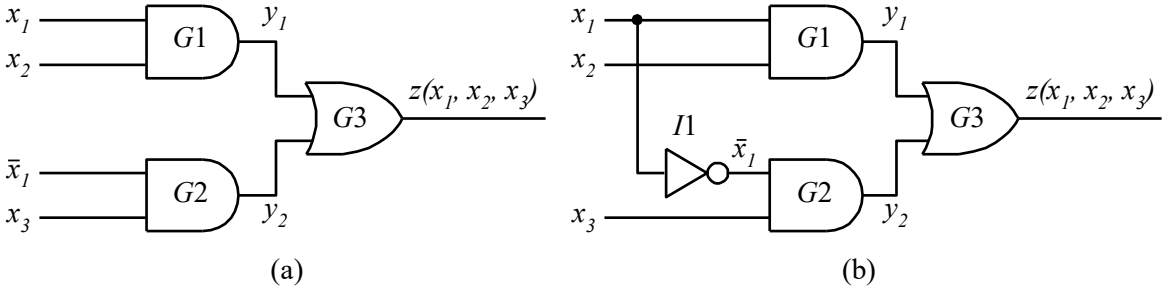
$y_1 = x_1 x_2 = 0$

$z = y_1 + y_2 = 1$



(c)

Sample1: Timing Analysis (cont'd)



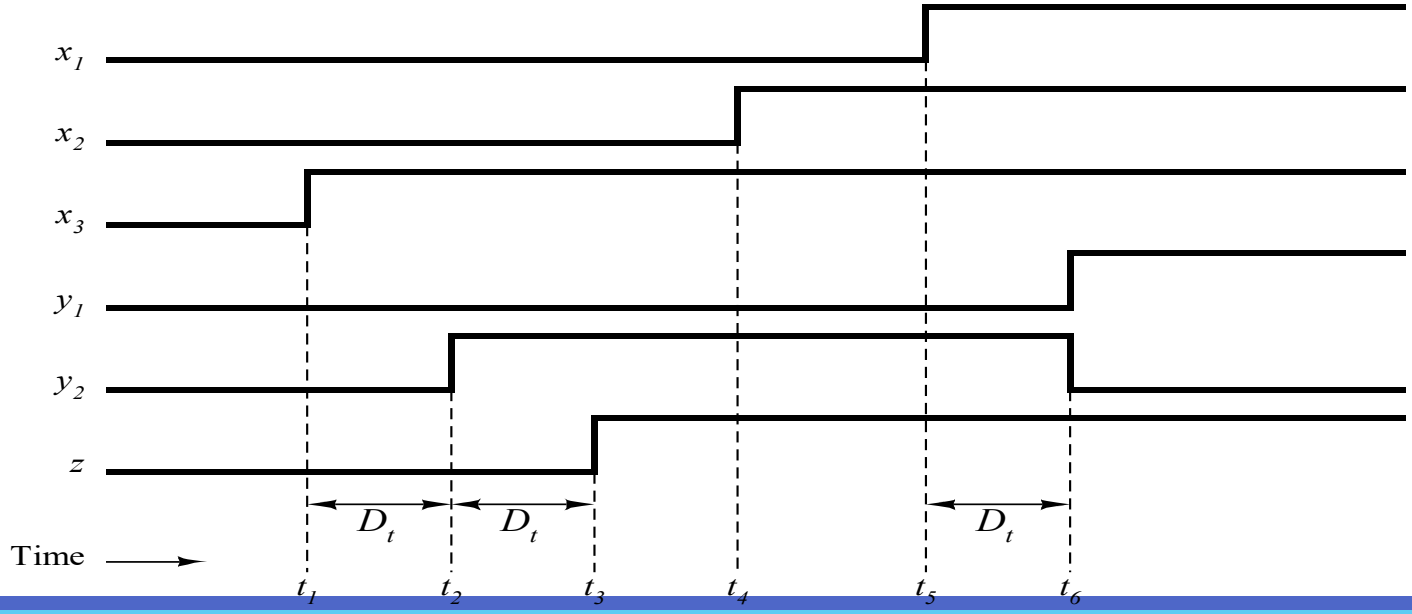
Initial values: $x_1x_2x_3 = 000$, $z = 0$

Input change t_5: x_1 0 -> 1

$y_1 = x_1 x_2 = 0$

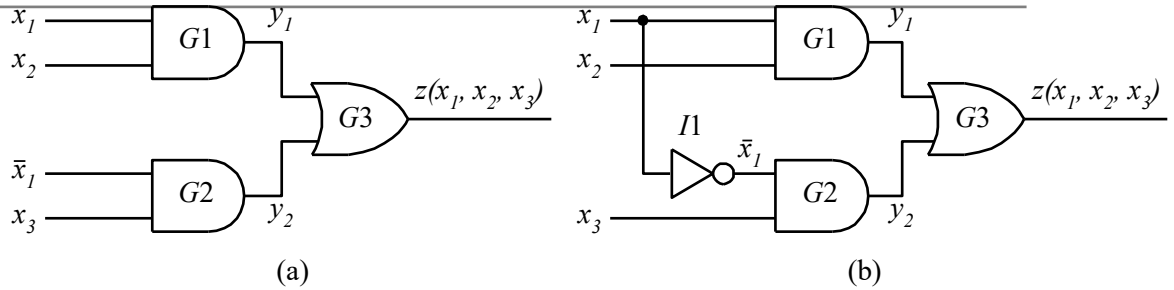
$y_2 = x'_1 x_3 = 1$

$z = y_1 + y_2 = 1$



Static Hazard: Sample 2

- G1 = Dt_1
- G2 = Dt_2
- G3 = Dt_3
- I1: 1 ns
- $Dt_1 > Dt_2 > Dt_3$

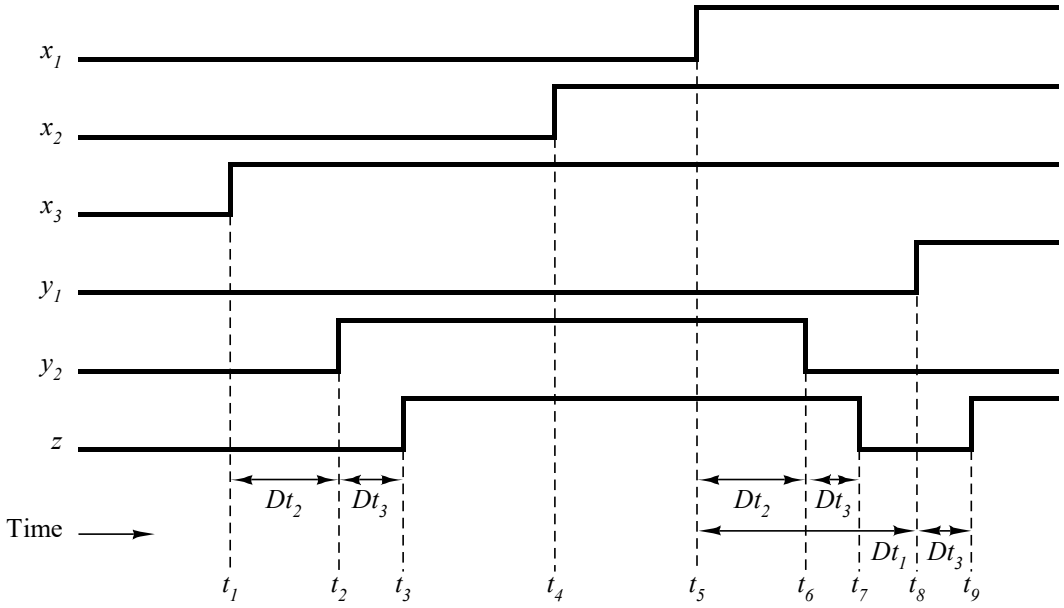


Initial values: $x_1x_2x_3 = 000$, $z = 0$

Input change t_1: x_3 0 -> 1, z=0

Input change t_4: x_2 0 -> 1, z=1

Input change t_5: x_1 0 -> 1, z=1



Sample 2 (cont'd)

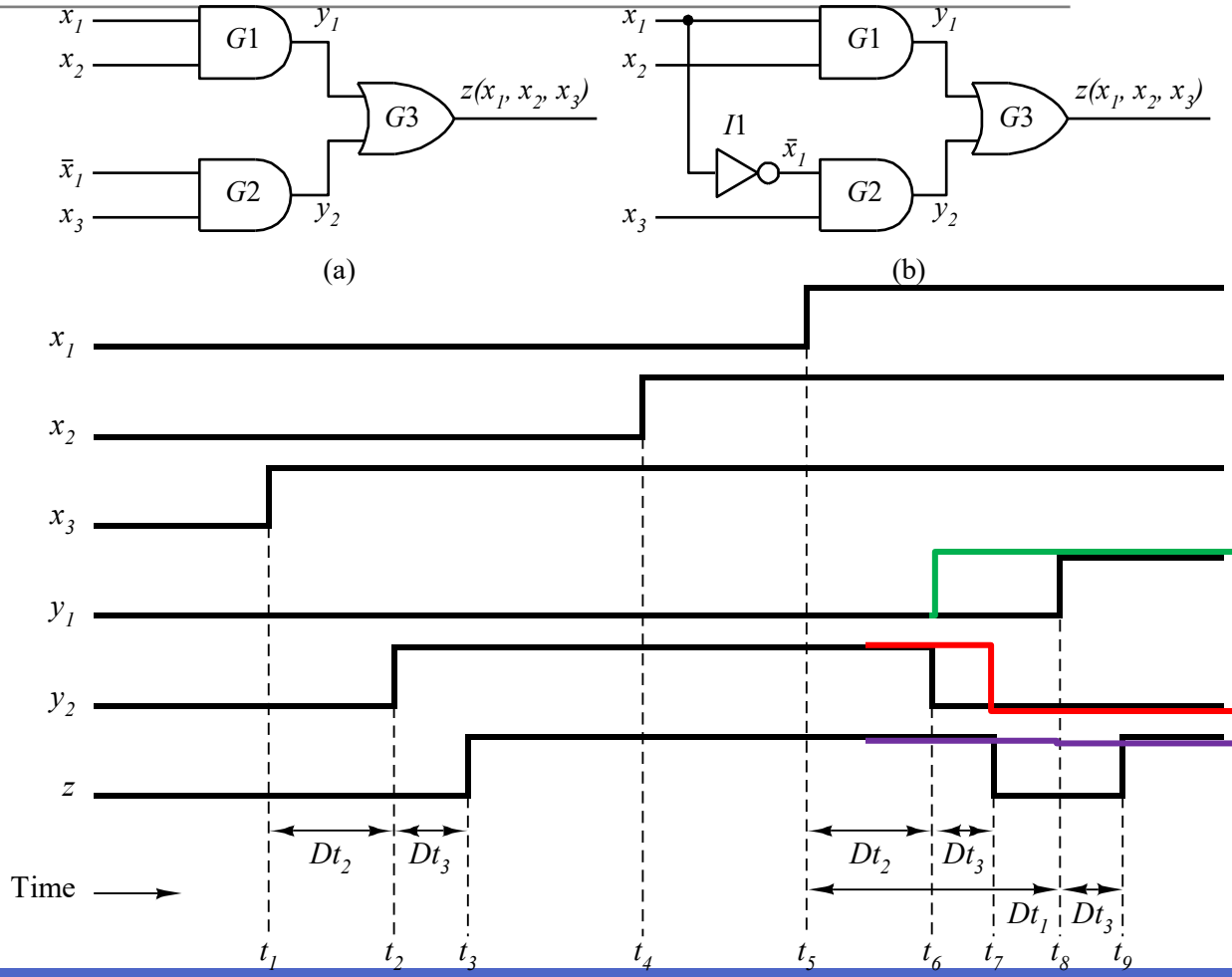
- G1 = Dt_1
- G2 = Dt_2
- G3 = Dt_3
- I1: 1 ns
- $Dt_1 < Dt_2$

Initial values: $x_1x_2x_3 = 000$, $z = 0$

Input change t_1: x_3 0 -> 1, z=0

Input change t_4: x_2 0 -> 1, z=0

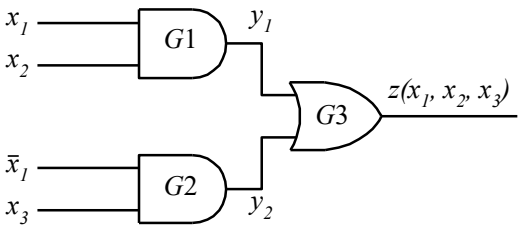
Input change t_5: x_1 0 -> 1, z=1



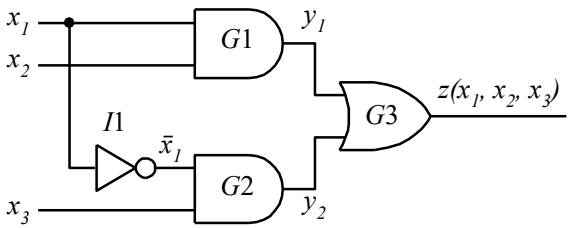
(d)

Sample 2 (cont'd)

- Delay
  - G1, G2, G3: 1 ns
  - I1: 0.5 ns



(a)



(b)

Initial values: $x_1x_2x_3 = 111$, $z = 1$

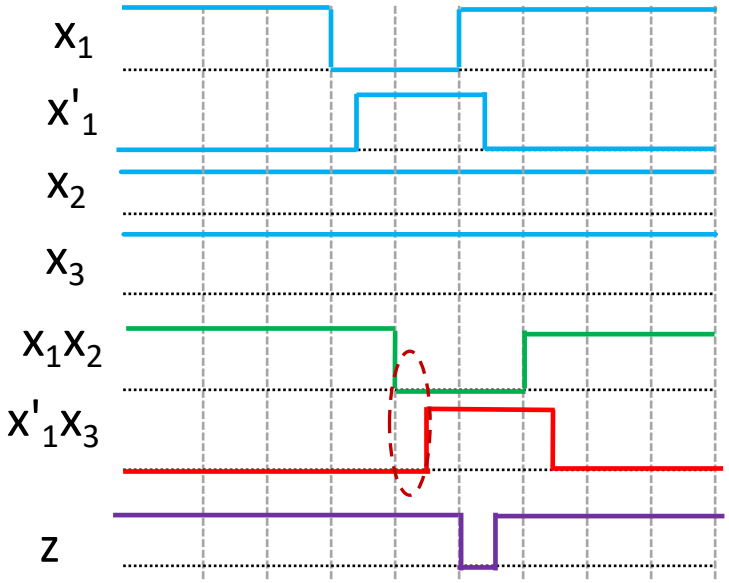
Next values: $x_1x_2x_3 = 011$, $z = 1$

T =1 $y_1 = x_1 x_2 = 1$

T =1.5 $y_2 = x'_1 x_3 = 0$

T =2 $z = y_1 + y_2 = 1$

T =2.5 $z = y_1 + y_2 = 1$



T = 1 $y_1 = x_1 x_2 = 0$

$y_2 = x'_1 x_3 = 0$

$z = 1$

T = 1.5 $y_1 = x_1 x_2 = 0$

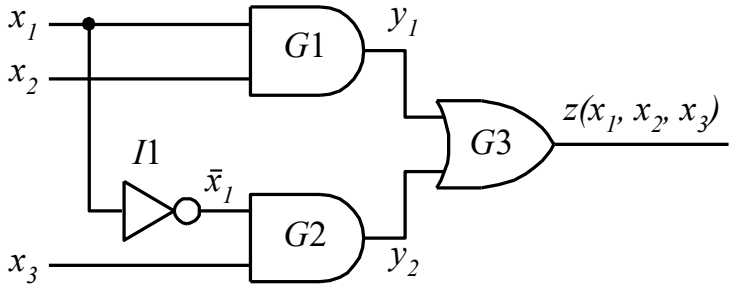
$y_2 = x'_1 x_3 = 1$

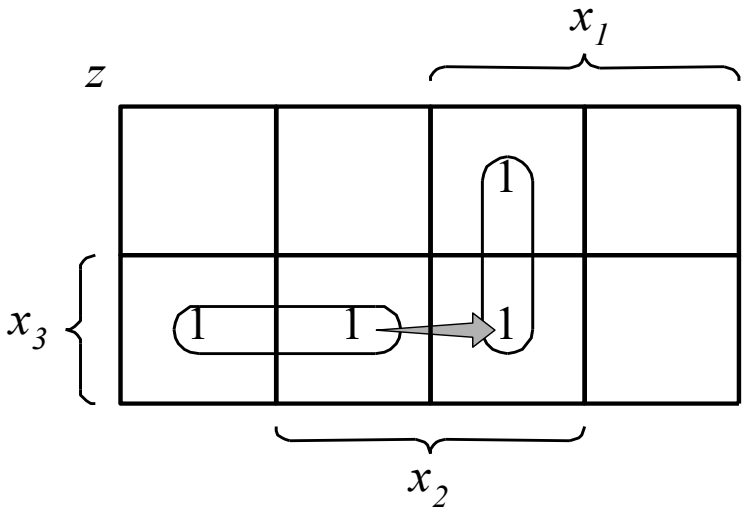
$z = 1$

T = 2.5 $z = y_1 + y_2 = 1$

Static Hazard & K-map

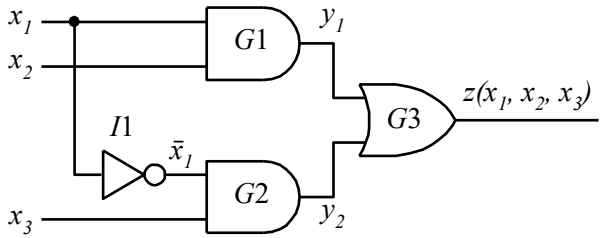
- Identifying hazards on K-map
  - (0,1,1) -> (1,1,1)
  - G1: 0 ->1 (faster)
  - G2: 1->0



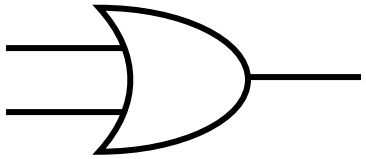


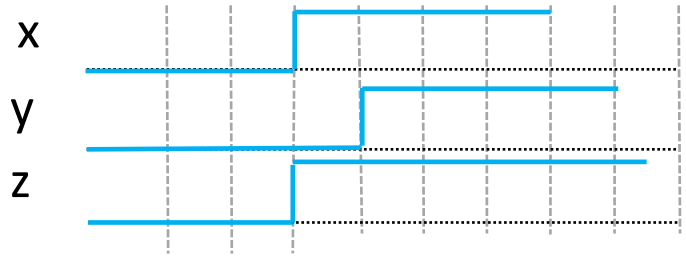
Static Hazard: AND-OR

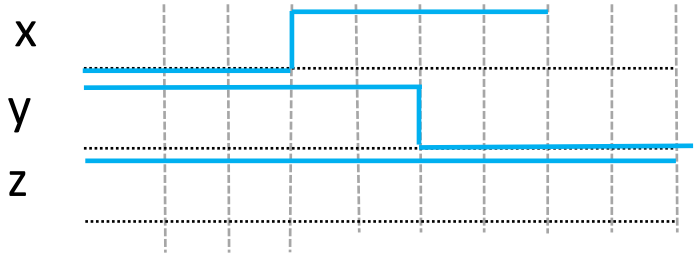
- AND Gates
  - literal or its complement
  - => No race
  - => No hazard
- OR Gates
  - Different paths
  - => race
  - => hazard
- Which Hazard?

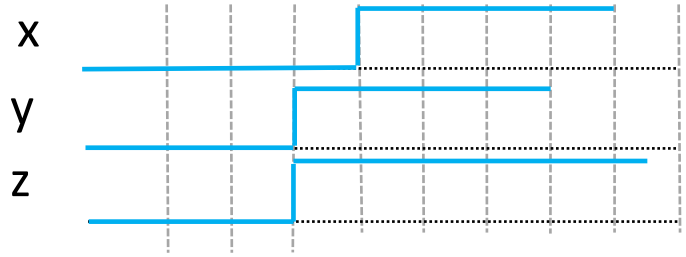


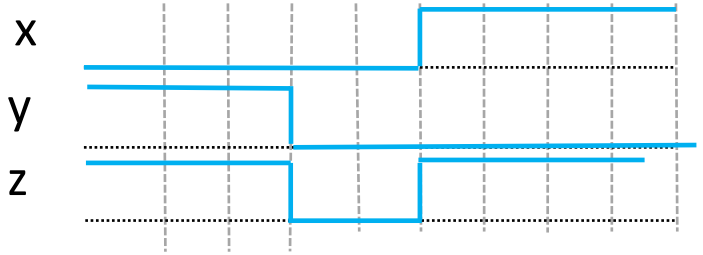
Static Hazard: OR











Static Hazard: AND-OR (cont'd)

- Two-level AND-OR Circuits
  - Static 0 hazards do not exist in the sum-of products (AND-OR) implementation
  - Static 1 hazards are possible
  - K-map of the function F in the previous example :
    - Cell 3 (011) and cell 7 (111) are covered in two product terms

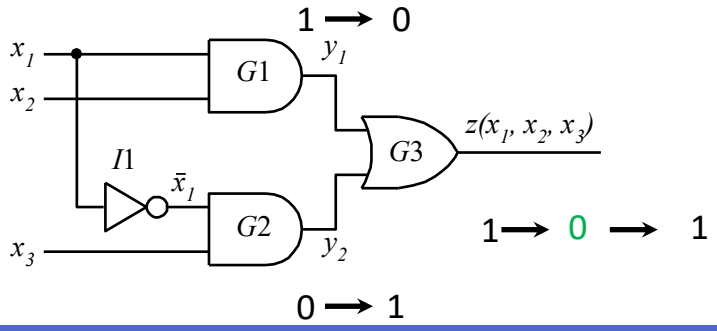
Initial values: $x_1x_2x_3 = 111$, $Z = 1$

$y_1 = x_1 x_2 = 1$

$y_2 = x'_1 x_3 = 0$

$z = y_1 + y_2 = 1$

Faster



Input change: x_1 1 -> 0

$y_1 = x_1 x_2 = 0$

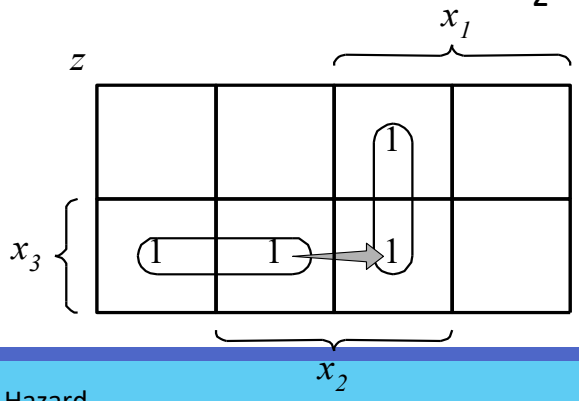
$y_2 = x'_1 x_3 = 0$

$z = y_1 + y_2 = 0$

$y_1 = x_1 x_2 = 0$

$y_2 = x'_1 x_3 = 1$

$z = y_1 + y_2 = 1$

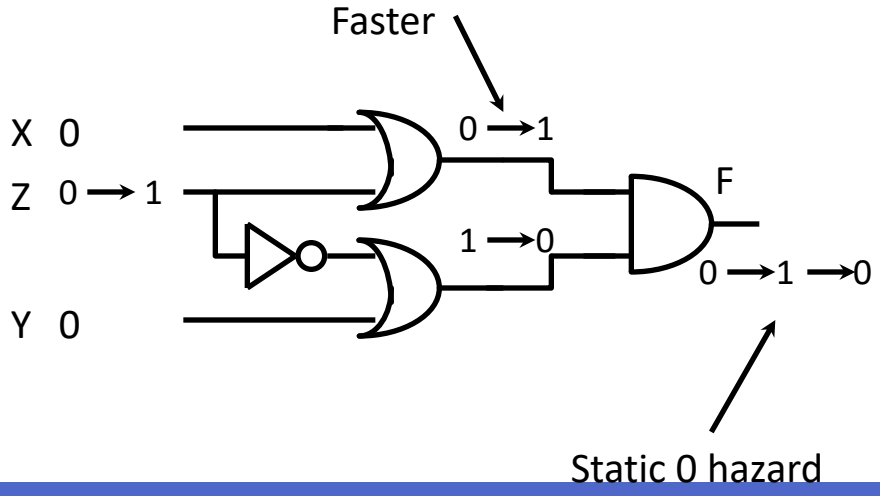


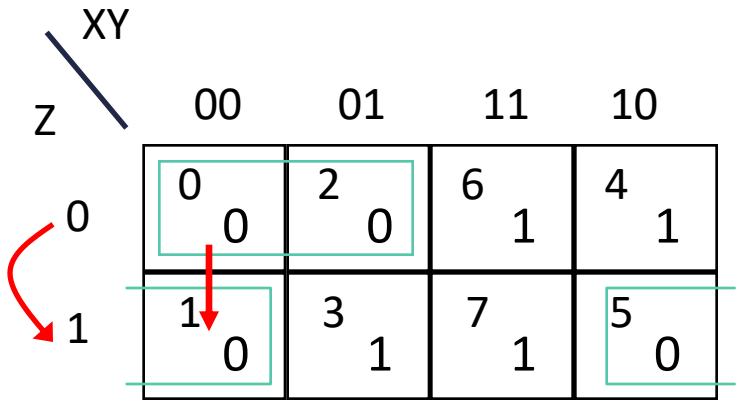
Static Hazard: OR-AND

- Two-level OR-AND circuits
  - Static 1 hazards do not exist in the products-of-sum (OR_AND) implementation
  - Static 0 hazards are possible
  - F = (x+z) (y+z')

Static Hazard: OR-AND (cont'd)

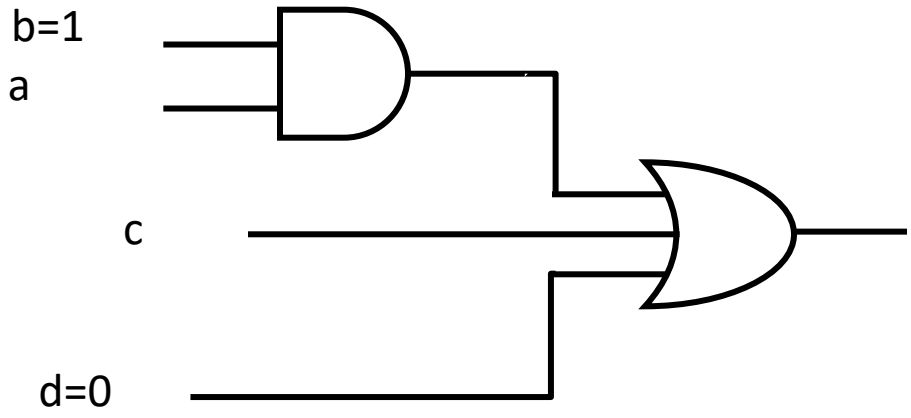
- Two-level OR-AND circuits
  - Static 1 hazards do not exist in the products-of-sum (OR_AND) implementation
  - Static 0 hazards are possible
  - F = (x+z) (y+z')
  - K-map of the function F in the previous example :
    - Cell 0 (000) and cell 1 (001) are covered in two sum terms





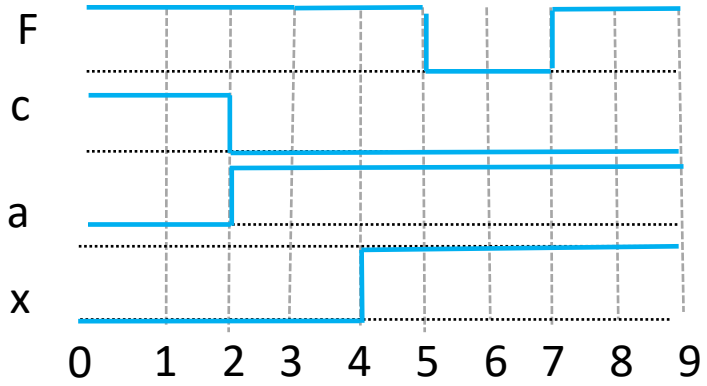
Static Hazard: Sample 3

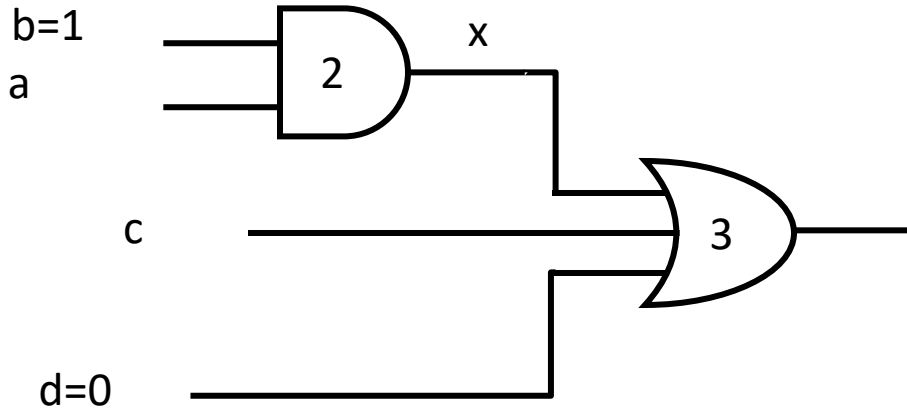
- Implement F = a.b + c + d
  - AND gate : 2 ns
  - Or gate: 3 ns



Static Hazard: Sample 3 (cont'd)

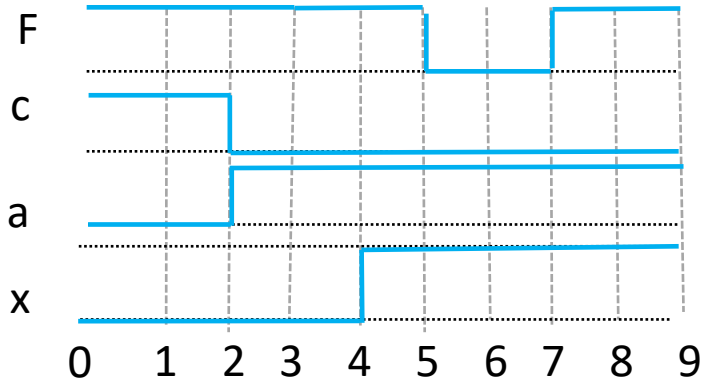
- Is there any hazard?

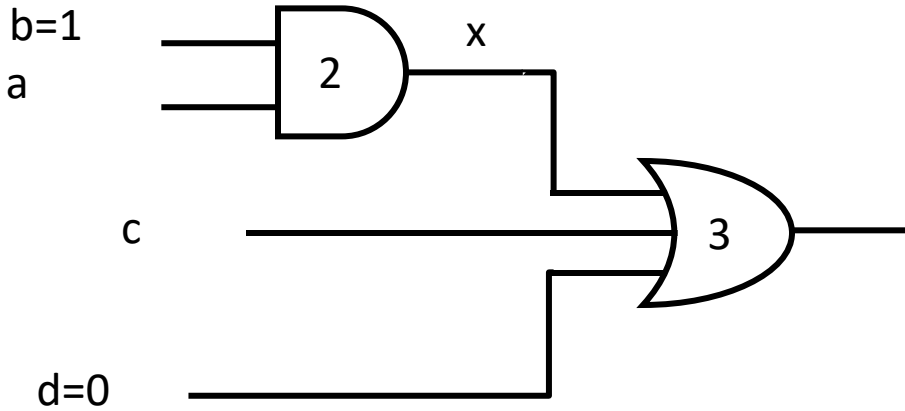




Static Hazard: Sample 3 (cont'd)

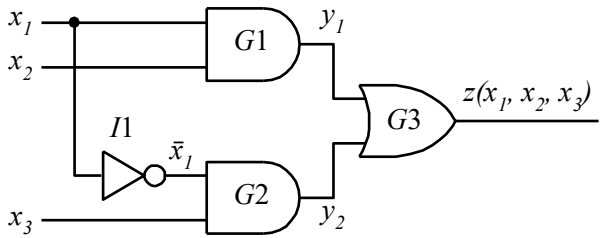
- Is there any hazard?
  - Yes
  - Due to changes in a and c signals at the same time
  - Called functional hazard





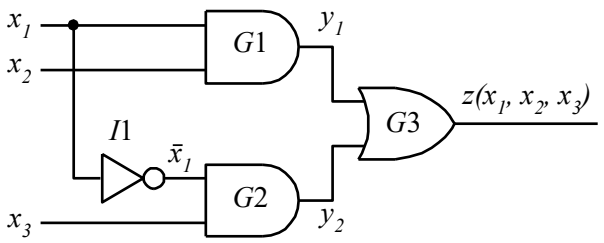
Static Hazard: Types

- Functional hazard
  - Changes in more than one input may cause hazard
- Potential hazard
  - Changes in only one input may cause hazard



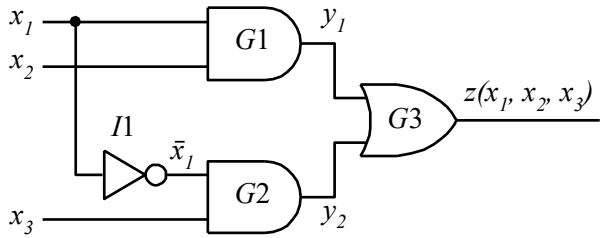
Static Hazard Free Circuits

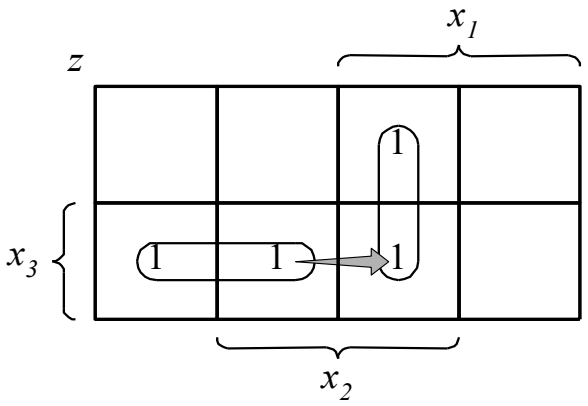
- Functional hazard
  - Design a circuit in such a way that **only one input** changes at each time
- Potential hazard
  - Make output **independent of the input change orders**



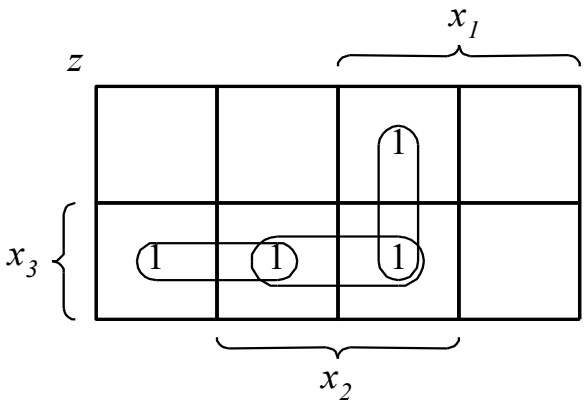
Static Hazard Free Circuits: Potential Hazards

- Make output **independent of the input change orders**
- Insert a gate
  - Its output does not change during G1 and G2 transition
  - Keeps the final output fixed during G1 and G2 transition
  - E.g., PT: x_2x_3 does not change during x1 changes





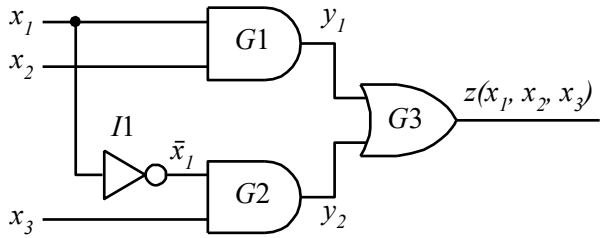
(a)

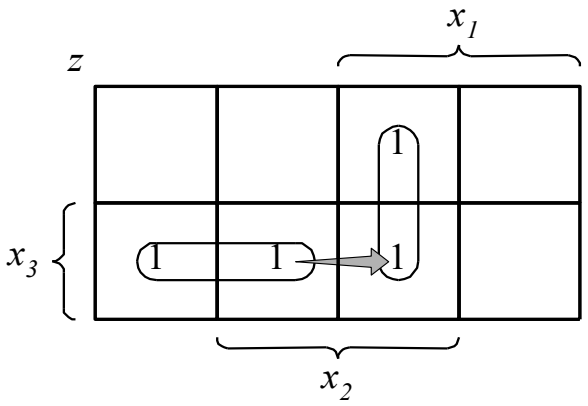


(b)

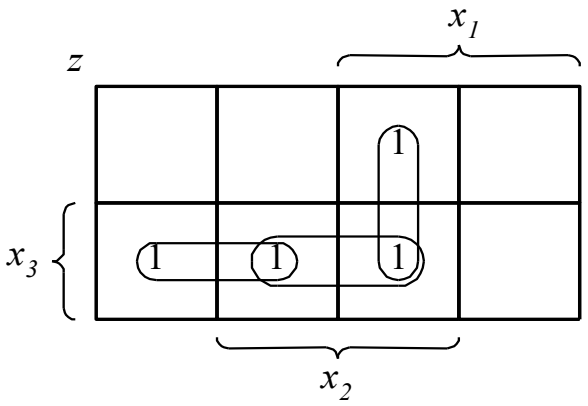
Static Hazard Free Circuits (cont'd)

- Hazard in K-map
  - Adjacent cubes
  - Its borders are not covered by any other cubes
- Hazard free in K-map
  - Covering each pair of adjacent cubes with a common product/sum term
  - =>Redundant gates
  - =>Non-minimum realization





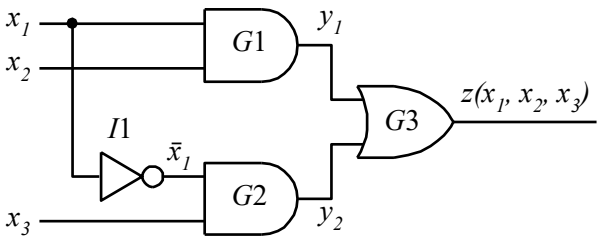
(a)

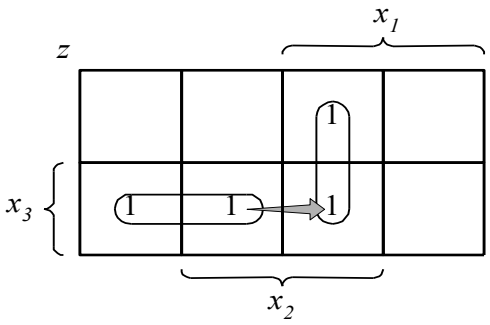


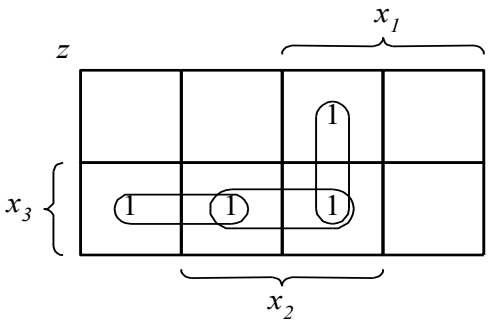
(b)

Static Hazard Free : AND-OR

- Two-level AND-OR circuits
  - Add a prime implicant that combines the two inputs that cause static 1 hazard
  - Consensus
  - Combine cell 3 (011) and cell 7 (111)
    - x_2x_3

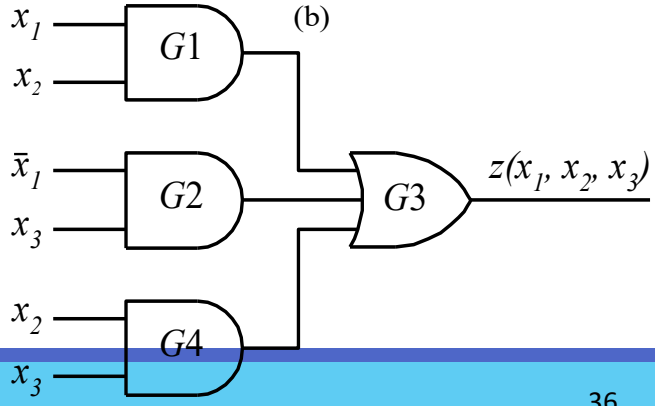






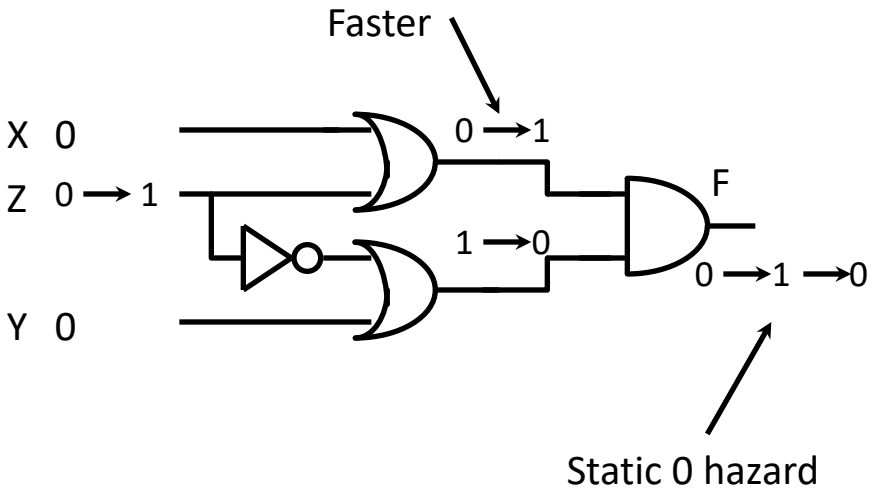
$F = (x_1x_2)+(x'_1x_3)$

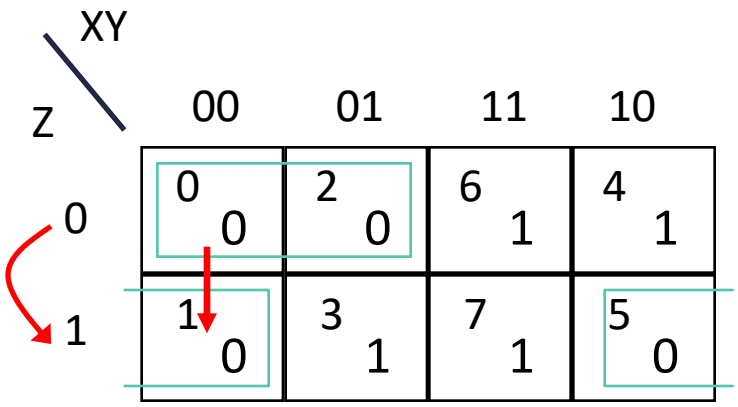
$F = (x_1x_2)+(x'_1x_3) + (x_2x_3)$



Static Hazard Free: OR-AND

- Two-level OR-AND circuits
  - Add a prime implicant that combines the two inputs that cause static 0 hazard
  - Consensus
  - Combine cell 0 (000) and cell 1 (001)
    - X+Y F = (X+Z)(Y+Z')

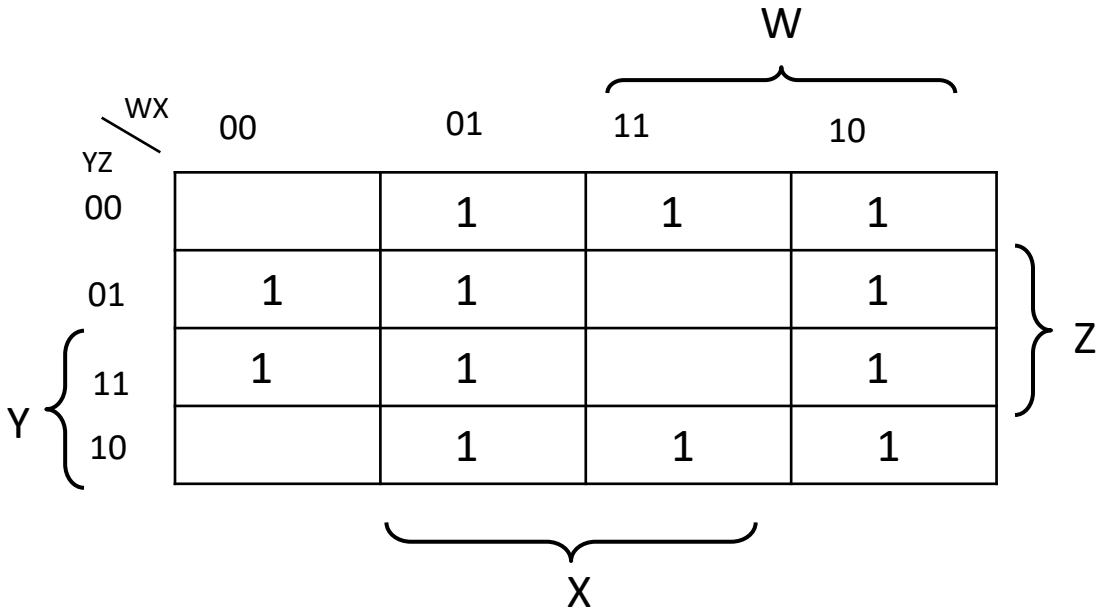




F = (X+Z)(Y+Z')(X+Y)

Static Hazard Free: Sample 4

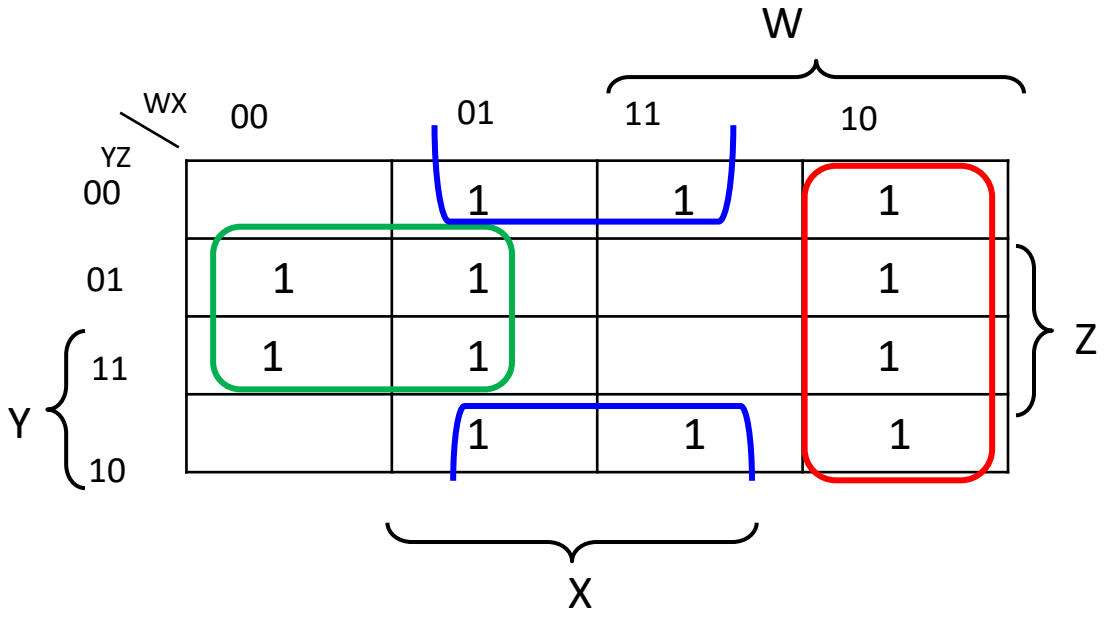
- Write minimal form for F
- Identify static-1 hazards
- Eliminate static-1 hazards



Static Hazard Free: Sample 4 (cont'd)

- Write minimal form for F

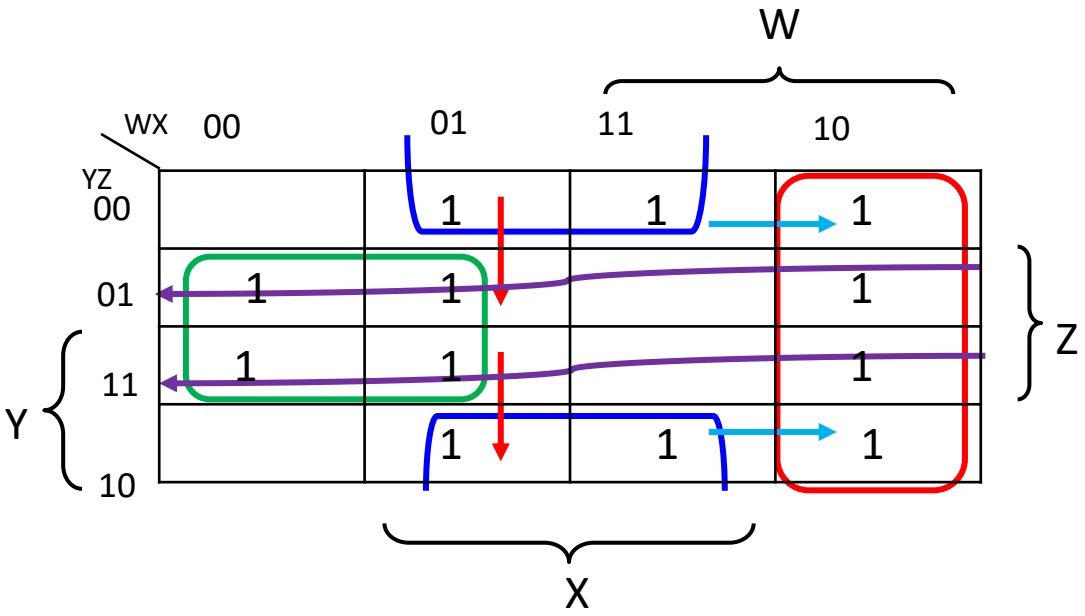
$F = W \bullet X' + W' \bullet Z + Z' \bullet X$



Static Hazard Free: Sample 4 (cont'd)

- Identify static-1 hazards
  - Changing Z from 0 to 1 or 1 to 0 may cause glitch
  - Changing X from 0 to 1 or 1 to 0 may cause glitch
  - Changing W from 1 to 0 or 1 to 0 may cause glitch

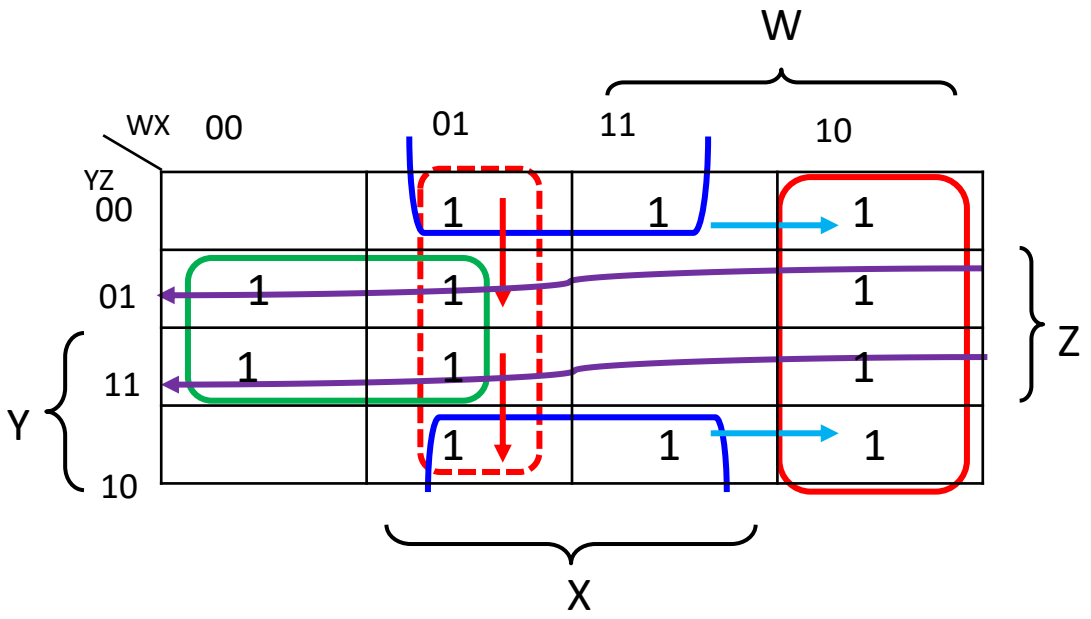
$F = W \bullet X' + W' \bullet Z + Z' \bullet X$



Static Hazard Free: Sample 4 (cont'd)

- Identify static-1 hazards
  - Changing Z from 0 to 1 or 1 to 0 may cause glitch

$$F = X \bullet W' + X' \bullet Z + Z' \bullet W$$
$$+ X \bullet W'$$

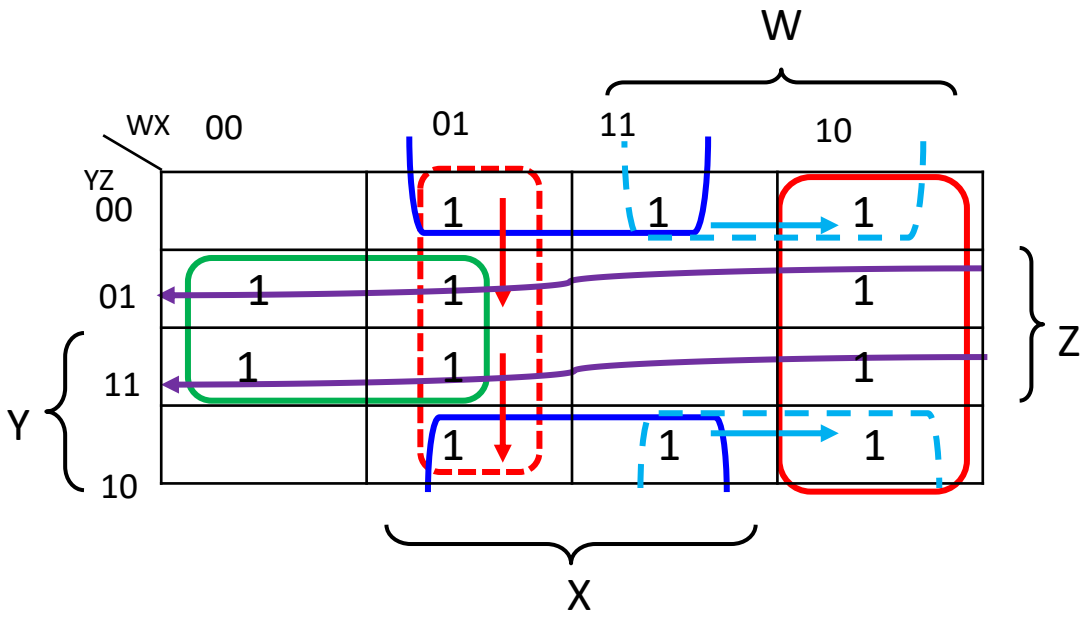


Static Hazard Free: Sample 4 (cont'd)

- Identify static-1 hazards
  - Changing Z from 0 to 1 or 1 to 0 may cause glitch
  - Changing X from 0 to 1 or 1 to 0 may cause glitch

$F = X \bullet W' + X' \bullet Z + Z' \bullet W$

$+ X \bullet W'$ $+ W \bullet Z'$



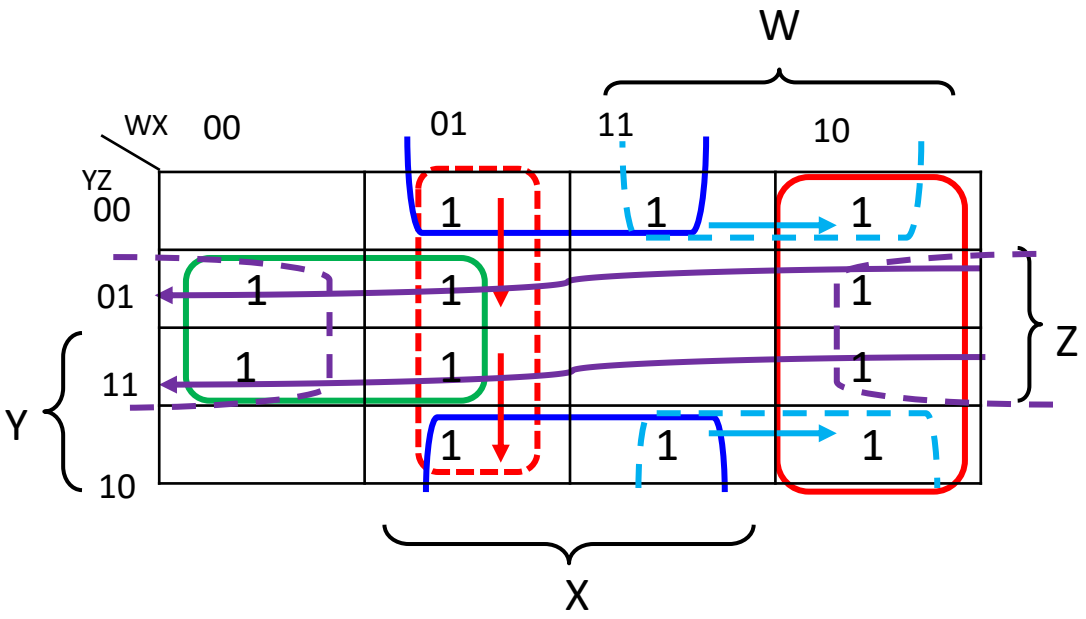
Static Hazard Free: Sample 4 (cont'd)

- Identify static-1 hazards
  - Changing Z from 0 to 1 or 1 to 0 may cause glitch
  - Changing X from 0 to 1 or 1 to 0 may cause glitch
  - Changing W from 1 to 0 or 1 to 0 may cause glitch

$F = X \bullet W' + X' \bullet Z + Z' \bullet W$

$+ X \bullet W'$ $+ W \bullet Z'$

$+ X' \bullet Z$



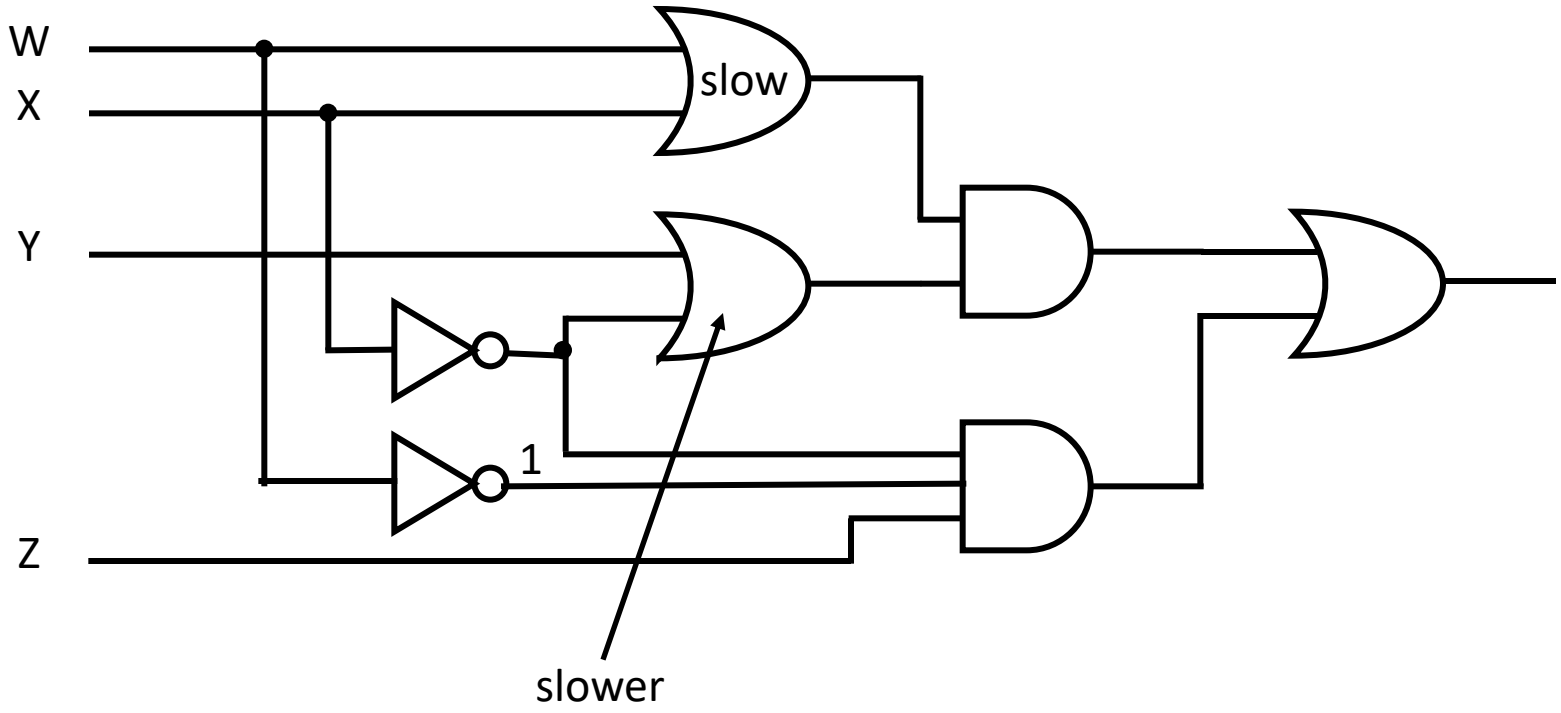
Dynamic Hazards

- Dynamic hazard (bounce)
  - Output changes multiple times during a change of state
  - Output changes more than once as a result of a single input change
  - (a) Dynamic 0 to 1 hazard
    - Output changes from 0 to 1 to 0 to 1
  - (b) Dynamic 1 to 0 hazard
    - Output changes from 1 to 0 to 1 to 0

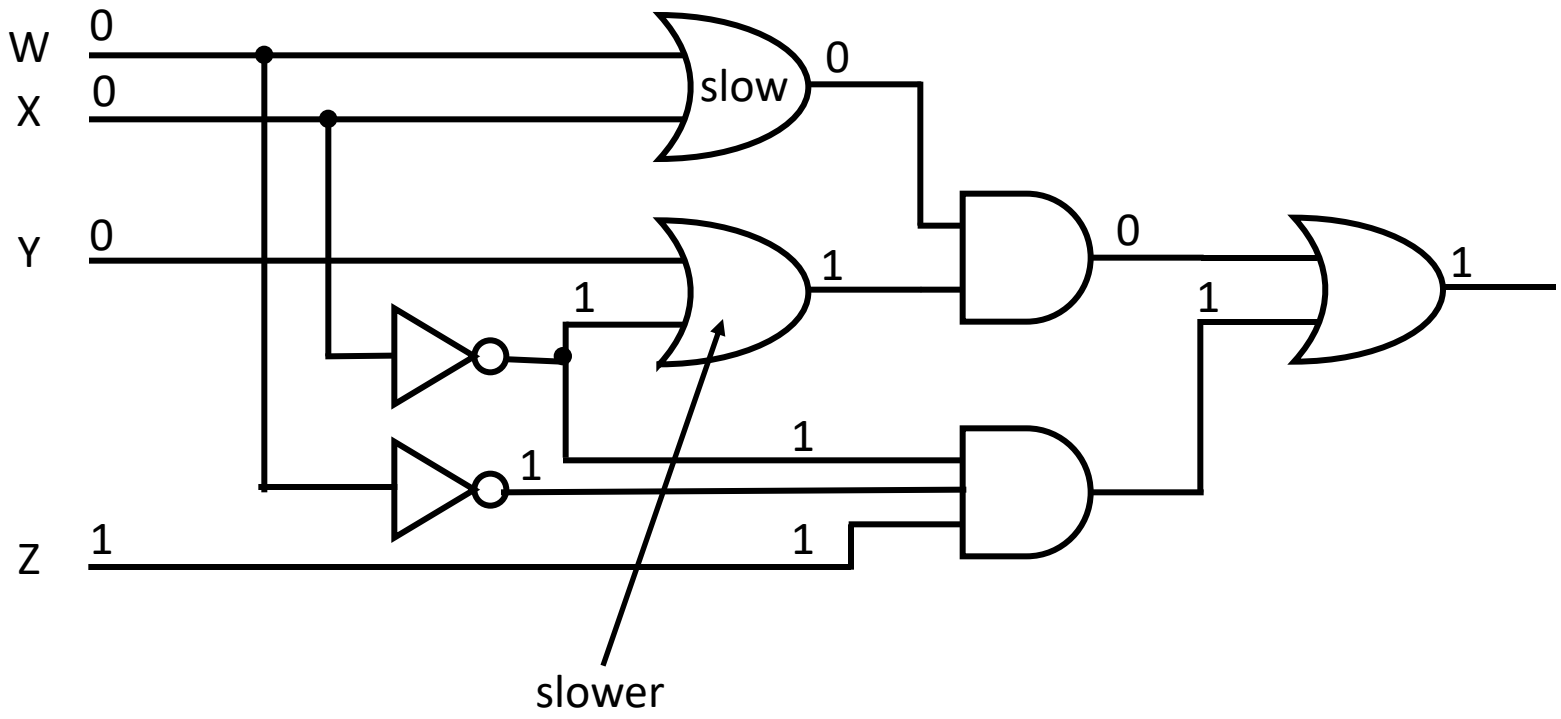
Why Dynamic Hazards?

- Existing multiple paths with different delays from the changing input to the changing output
- Static hazard

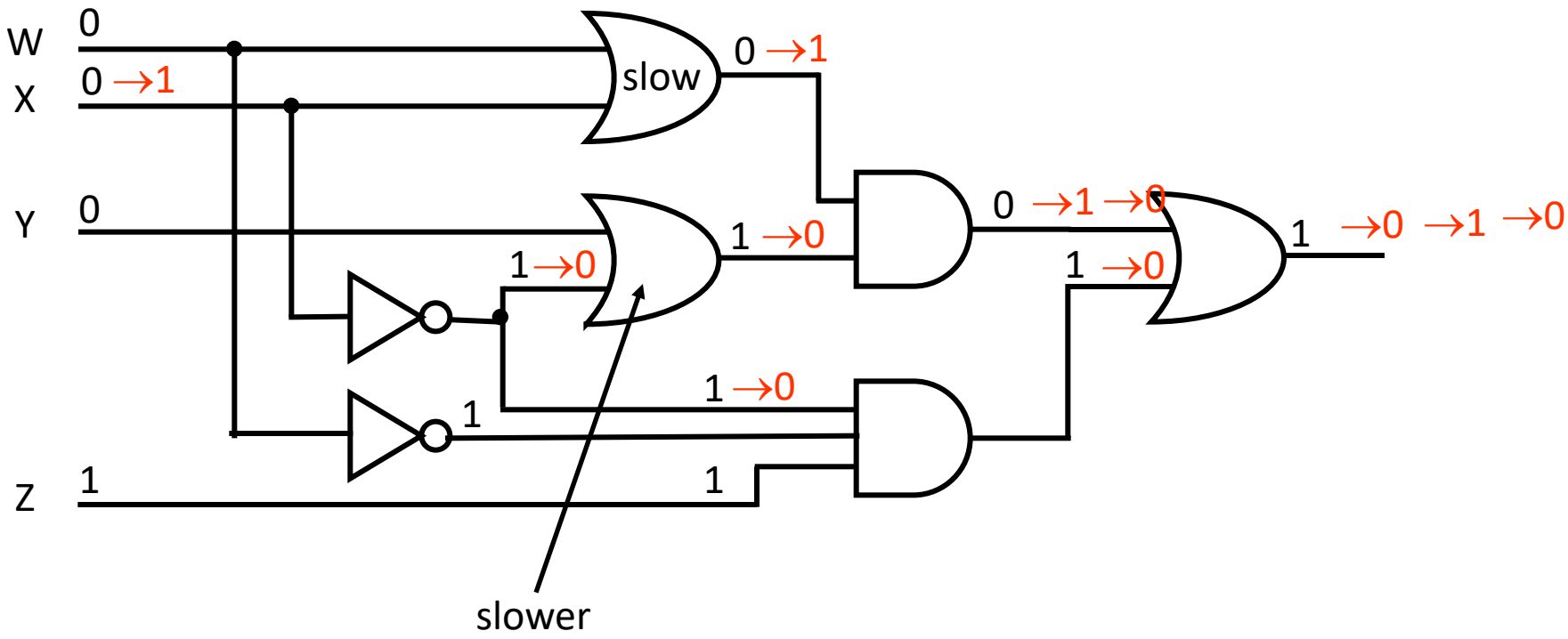
Dynamic Hazards: Sample



Sample (cont'd)



Sample (cont'd)



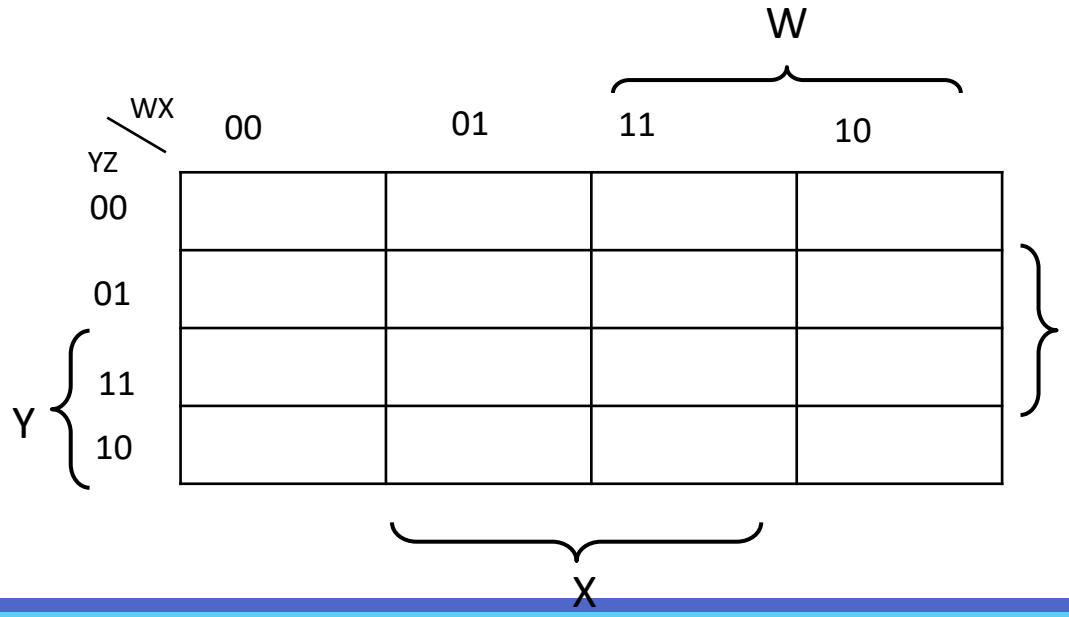
Dynamic Hazard Free?

- How to make a circuits dynamic hazard free?
  - Static hazard free networks
  - Properly designed two level AND-OR or OR-AND circuits.
    - A two level AND-OR or OR-AND circuit is properly design if a variable and its complement are never input to the same first level gate.
  - It may occur in multilevel circuits.

Sample 6

- Write minimal form for F
- Identify static-1 hazards
- Eliminate static-1 hazards

F(W,X,Y,Z) = $\sum m(1,2,3,12,13,14,15) + d(5,7)$

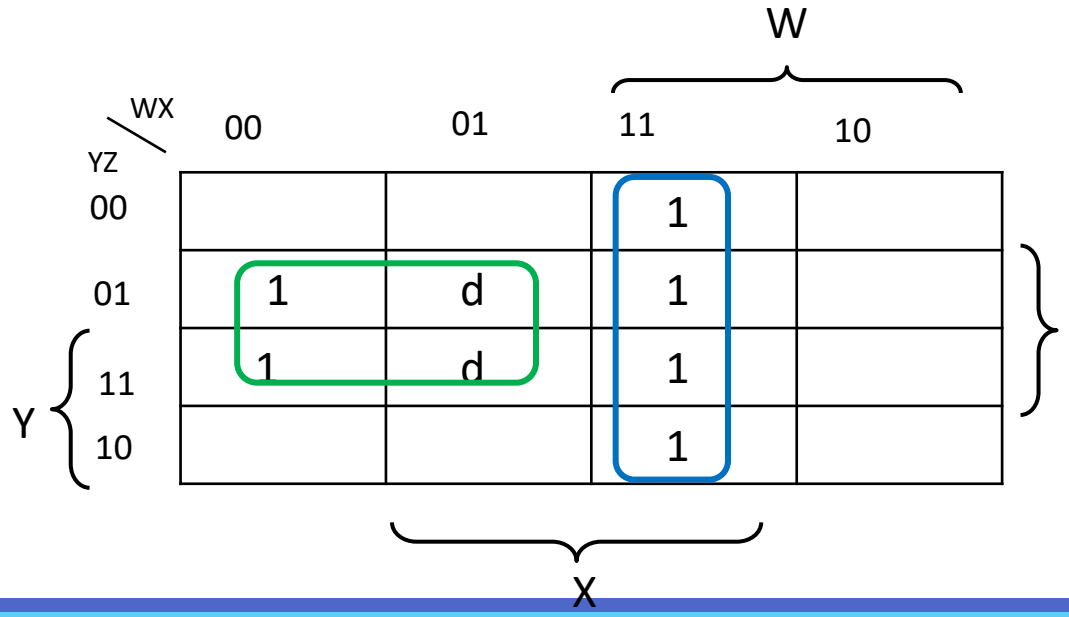


Sample 6 (cont'd)

- Write minimal form for F

F(w,x,y,z) = $\sum m(1,2,3,12,13,14,15) + d(5,7)$

F(w,x,y,z) = W'Z + WX

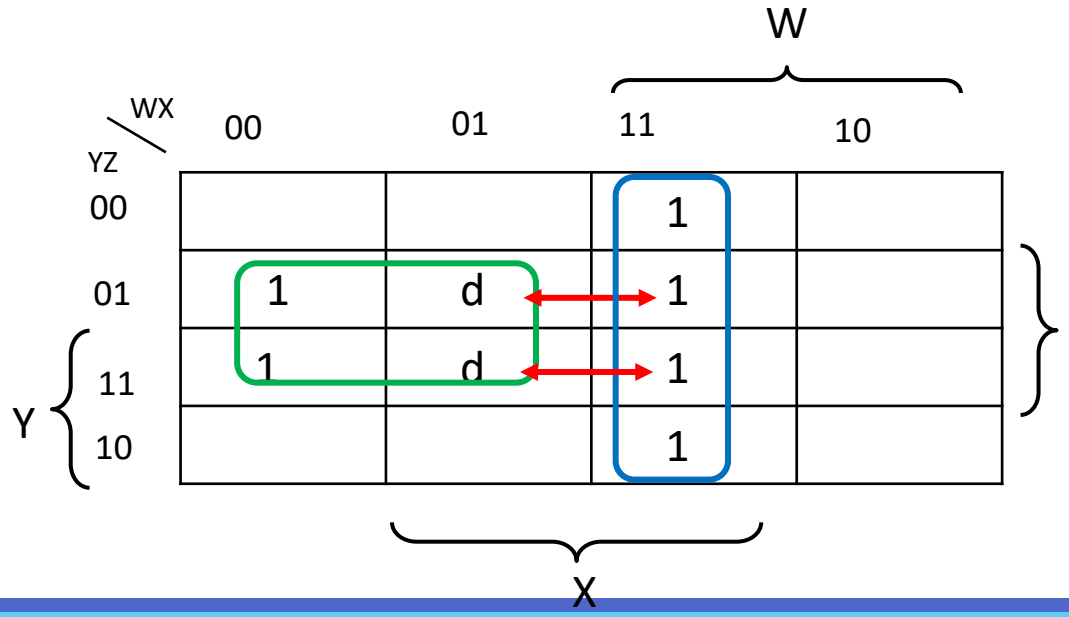


Sample 6 (cont'd)

- Identify static-1 hazards

F(w,x,y,z) = $\sum m(1,2,3,12,13,14,15) + d(5,7)$

F(w,x,y,z) = W'Z + WX

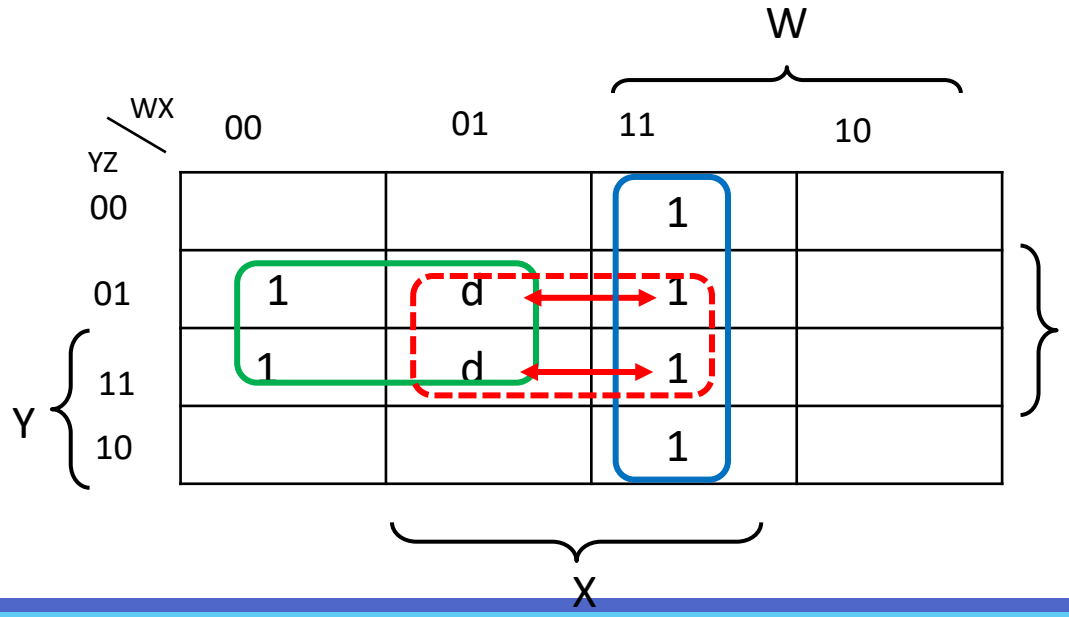


Sample 6 (cont'd)

- Eliminate static-1 hazards

F(w,x,y,z) = $\sum m(1,2,3,12,13,14,15) + d(5,7)$

F(w,x,y,z) = W'Z + WX + XZ

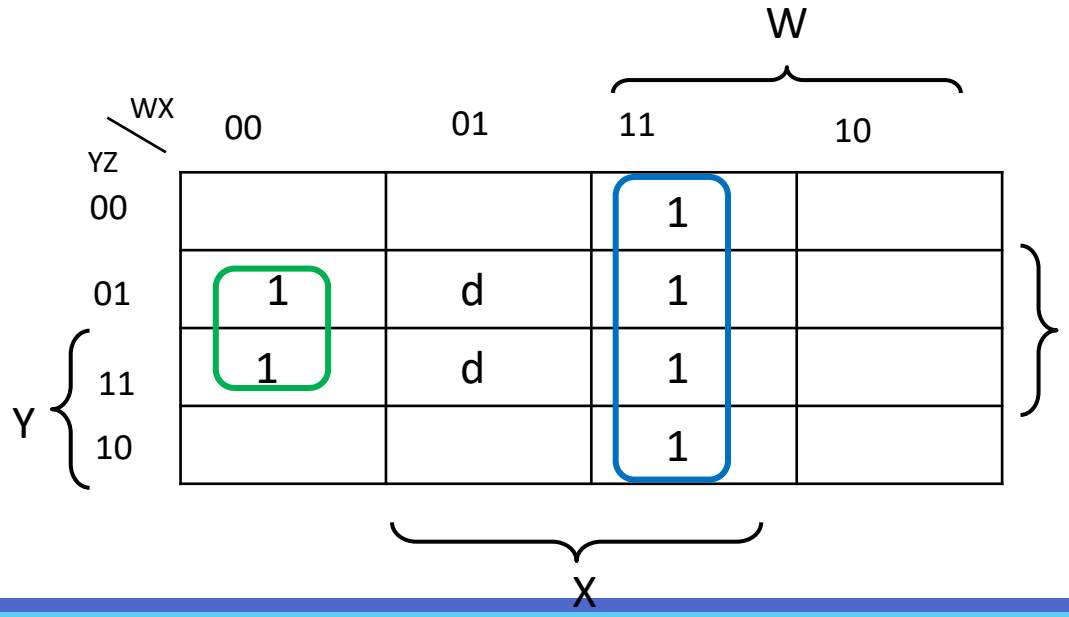


Sample 6 (cont'd)

- Eliminate static-1 hazards

F(w,x,y,z) = $\sum m(1,2,3,12,13,14,15) + d(5,7)$

F(w,x,y,z) = W'X'Z + WX



Summary

- Static Hazard
  - A properly designed two-level SOP (AND-OR) circuit
    - Has no static-0 hazards
    - It may have static-1 hazards
  - A properly designed two-level POS (OR-AND) circuit
    - Has no static-1 hazards
    - It may have static-0 hazards

- Dynamic Hazard
  - Do not occur in properly designed two-level SOP (AND-OR) or two-level POS (OR-AND) circuits

Summary (cont'd)

- Hazard analysis and elimination are typically needed in the design of asynchronous sequential circuits

- Hazard-free realization
  - Use the **complete sum or complete product**.
  - Do **not cover** don't cares.

Thank You