Digital Logic Circuit Design

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IRAN University of Science and Technology

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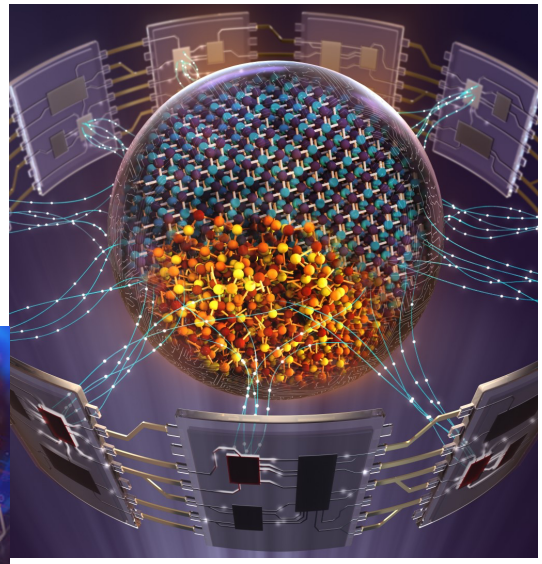
A Little About Me

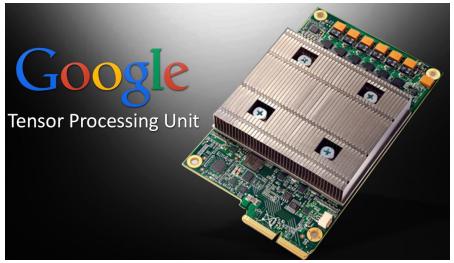
- Hajar Falahati
  - **Assitant Professor** @ Iran University of Science and Technology (**IUST**), since Sep. 2018.
  - **Postdoc** @ Institute in Fundamental Science and Technology (**IPM**), Dec 2016 – Sep 2018.
    - Supervised by *Prof. Hamid Sarbazi-Azad*, Prof. *Pejman Lotfi-Kamran*
  - **Research Visitor** @ University of Southern California (**USC**), Apr 2015 – Apr 2016.
    - Supervised by *Prof. Masoud Pedram* and *Prof. Muralli Annavaram*
  - **PhD** @ Sharif University of Technology (**SUT**), Sep 20111 – Oct 2016.
    - Supervised by *Prof. Shaahin Hessabi*
  - **Msc** @ Sharif University of Technology (**SUT**), Sep 2009 – Sep 2011
    - Supervised by *Prof. Shaahin Hessabi*
  - **BSc** @ Isfahan University of Technology (**IUT**), Sep 2005 – Sep 2009
    - Supervised by *Prof. Kiarash Bazargan and Mr. Nikaean*.

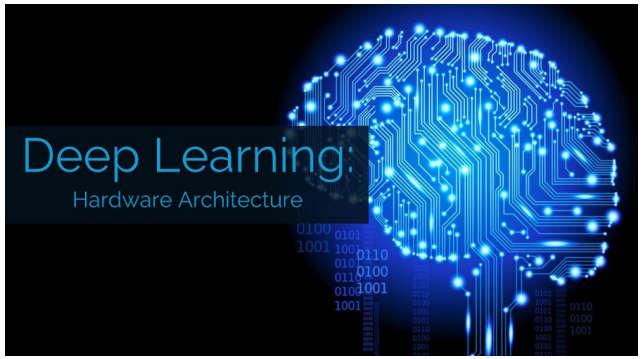
A Little About Me

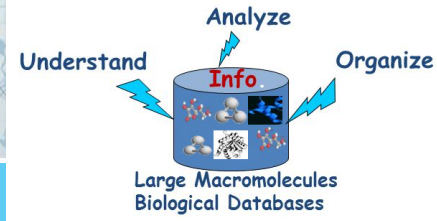
Iran University of Science & Technology
IUST

- Research Area
  - Hardware Accelerators
  - Neural Networks
  - GPU Architecture
  - Processing-in-Memory
  - Bioinformatics



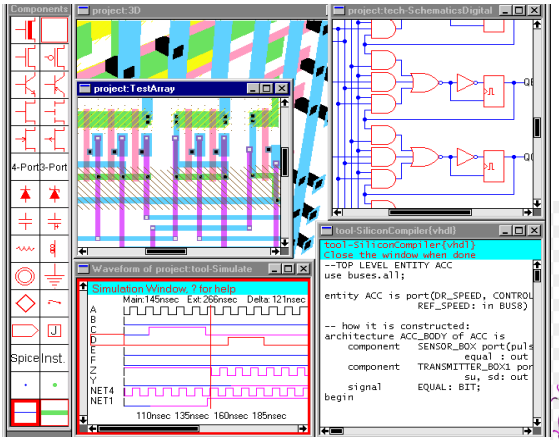


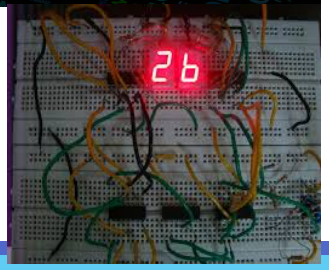




Course Information

- Digital Logic Circuit Design





Course Objective

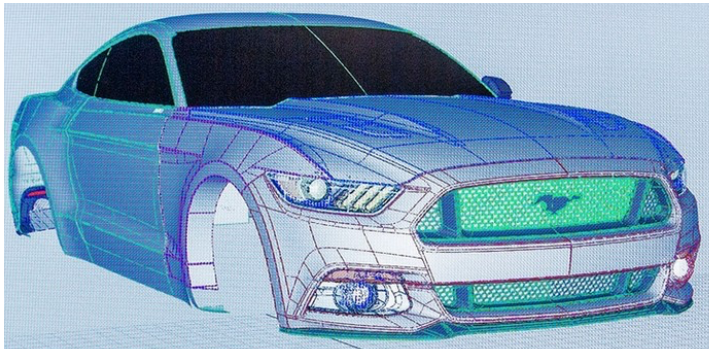
- **Digital system concepts**
  - Digital systems
  - Digital information

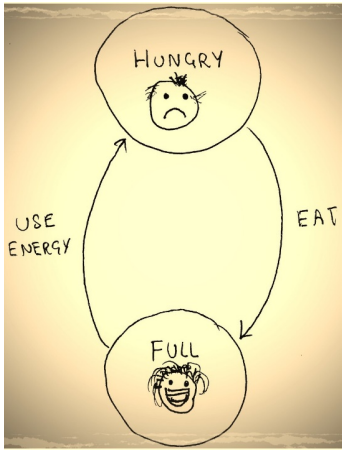
Course Objective (cont'd)

- **Digital storage**
  - Register
  - Memory

Course Objective (cont'd)

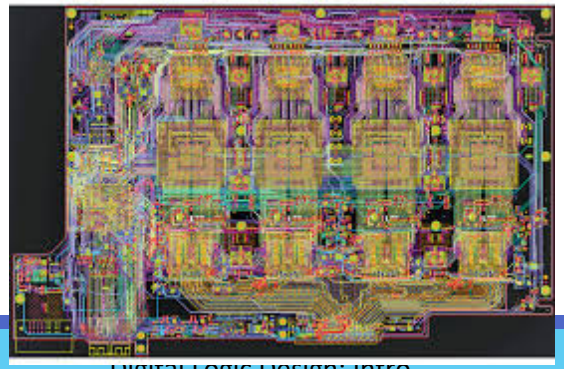
- **Digital system modeling**
  - Understand the system behavior





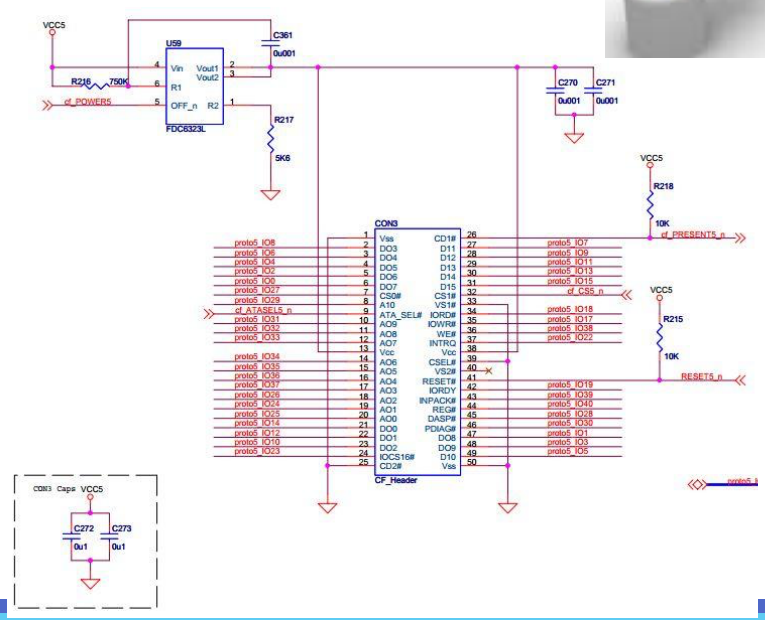
Course Objective (cont'd)

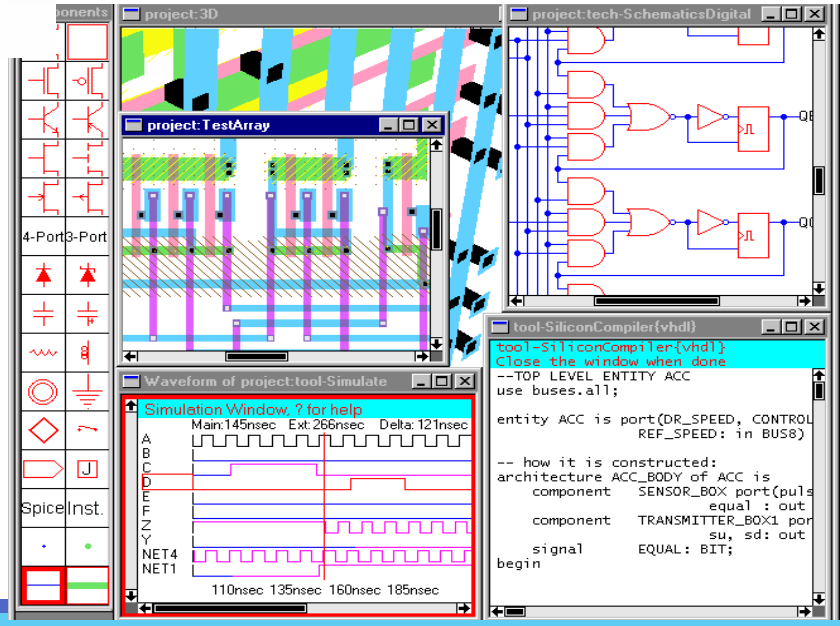
- **Digital system design**
  - **Simple** digital systems
  - **Complex** digital systems



Course Objective (cont'd)

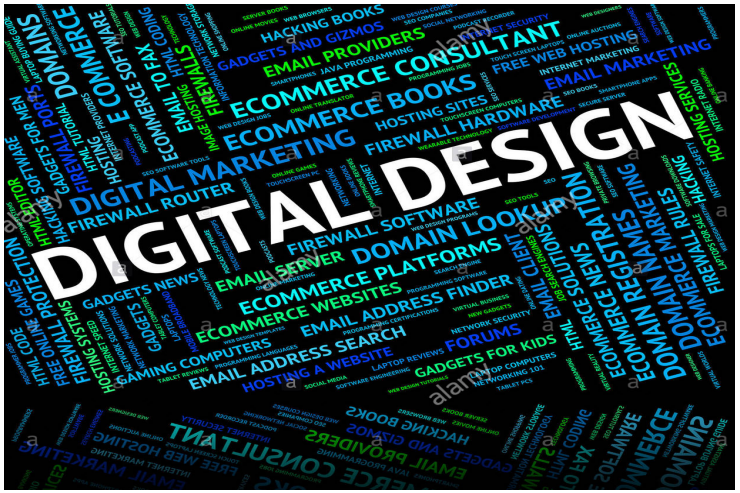
- **Design and simulation tools**
  - **Proteus**
  - **ISE**
  - **Quartus**





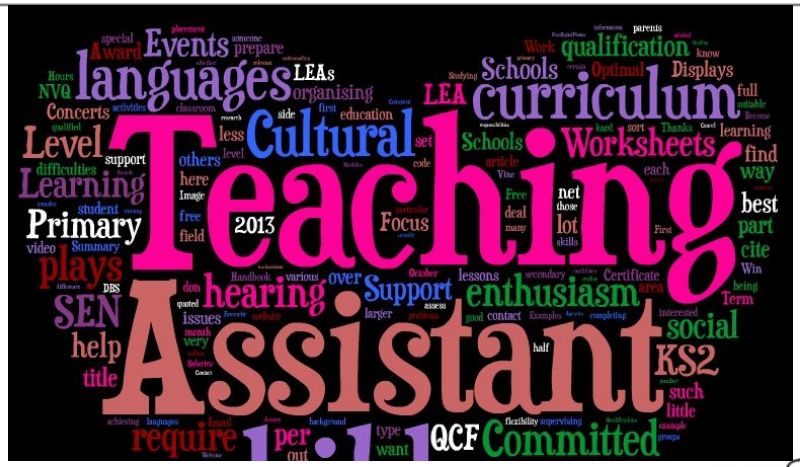
Class Information

- Class hour
  - Sat & Mon: 08:00-10:00.
- Instructor
  - Hajar Falahati
- Contact info
  - 313 CE, **IUST**
  - Office hour
    - Check my schedule on my office door



Teaching Assistant

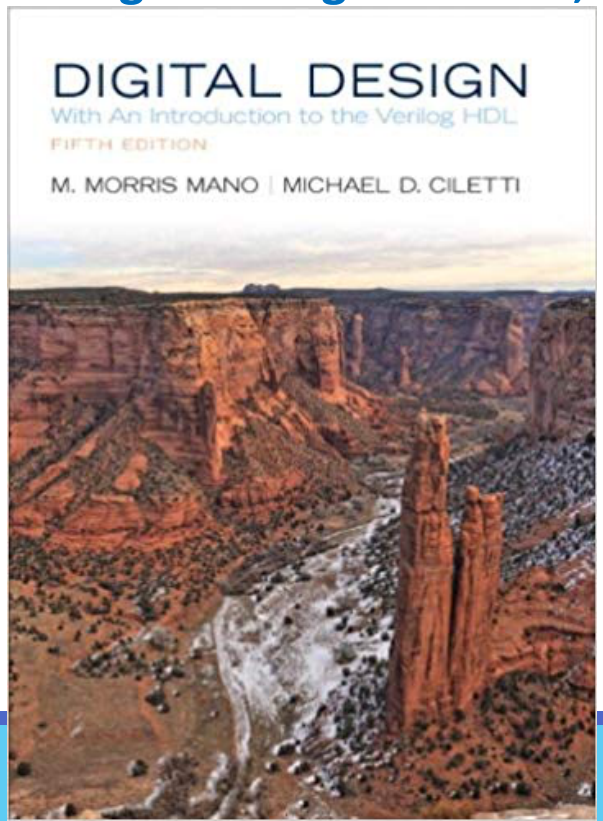
- TA team
  - Sepehr Babapour
  - Sana Shoeibi
  - Zahra Hosseini
  - Tohid Abedini
  - Mahsa Meimari
  - MirHosseing Seyed Nasiri

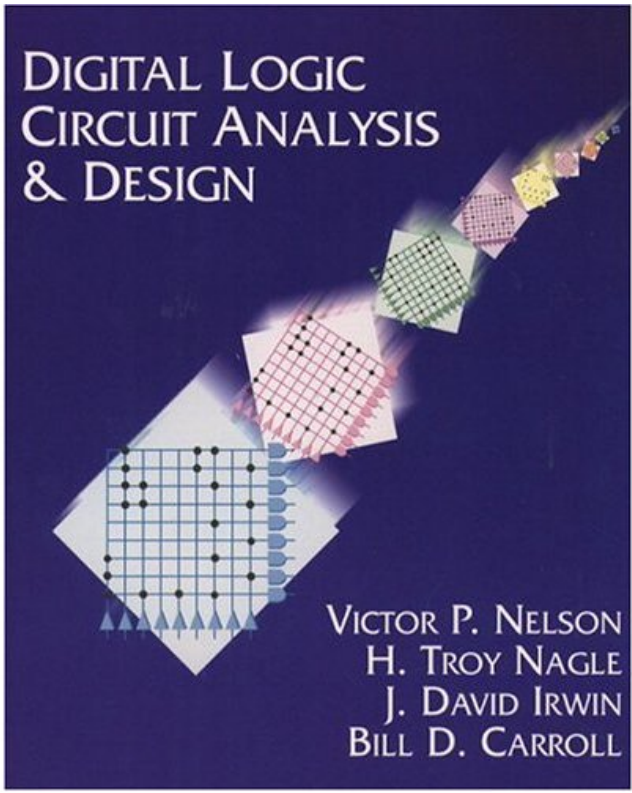


- Class TA hour
  - Tuesday 12:00 – 13:00

References and Copyright Notice

- **Digital Logic Circuit Analysis and Design**, by **Nelson, Nagle, Carroll and Irwin**
- **Digital Design, fifth edition,** by **Moris Mano**
- **Digital Design Lectures,** from **MIT, SUT, ETH, ..**





Class Policy

- Attend the class **on time**
  - Sat & Mon: 08:00 AM ~ 10:00
  - Class -121

- Cell Phones **off** or on **silent**

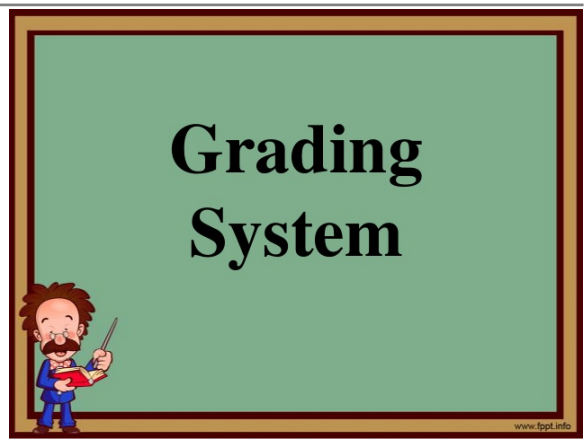
- Food **no, Water yes!**

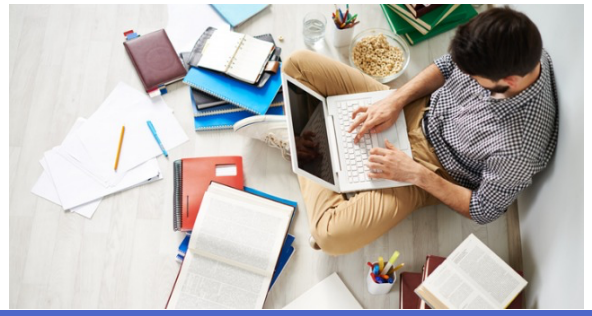
- Ask Questions **anytime**
  - Don't hesitate to ask even stupid questions!!!

- Pass me your **feedback/thought**
  - Anything related to the course

Grading

- Final Exam: 30%
- Midterm Exam: 20%
- Quiz: 10%
  - Four *scheduled* quizzes
  - TA class quizzes
- Class attendance: 10%
  - Lecture class
  - TA class
- Assignments & Project: 30%
  - Bonus points for outstanding projects



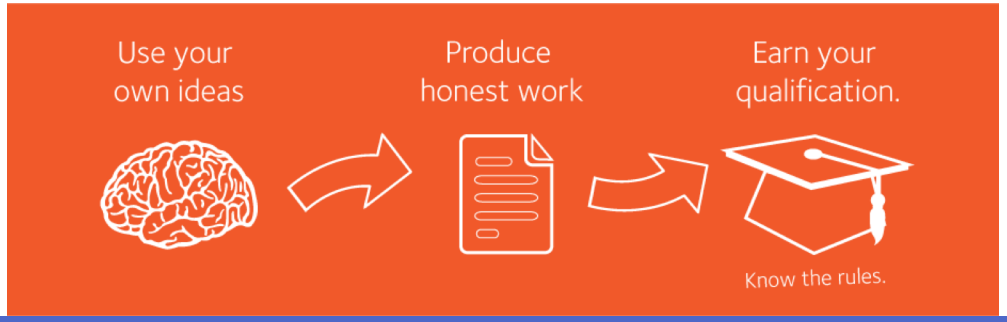


Assignments

- Deadlines
  - **Tight**
  - 3 days late is **allowed**!
  - > 3 days → **zero score**

- Discussion is **allowed**

- Copied assignments and academic misconduct is **zero score**



Academic Misconduct

- Using someone else's output
- Borrowing code from someone who took course before or has done the project
- Cheating in exams and assignments

Evaluation Policies

- Exam contents
  - Topics of this **Class** and **TA Classes**

- Grading Rules
  - You must achieve **50%** of assignments, **50%** of project, **50%** of midterm, and **50%** of final Exam scores.
  - You must also deliver at least **80%** of assignments.

Projects (cont'd)

- Project team:
  - 1 student!

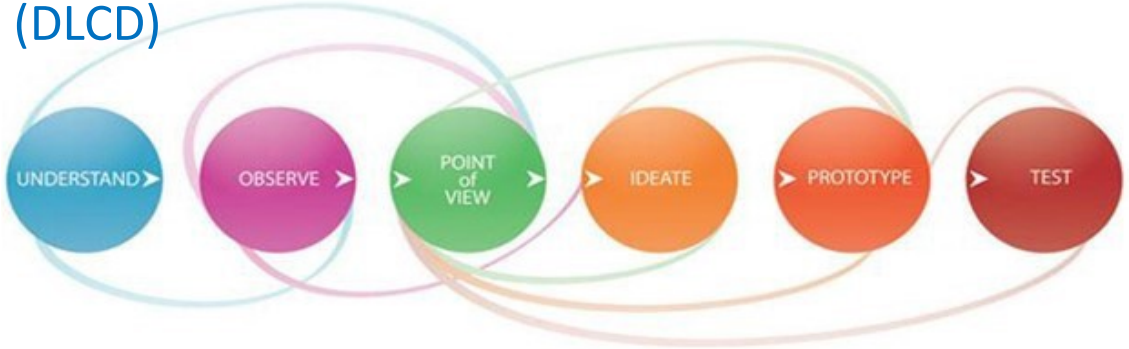
- Phases
  - Topic selection
  - Specification
  - Modeling
  - Block Diagram
  - Synthesis
  - Implementation
  - Documentation
  - Presentation

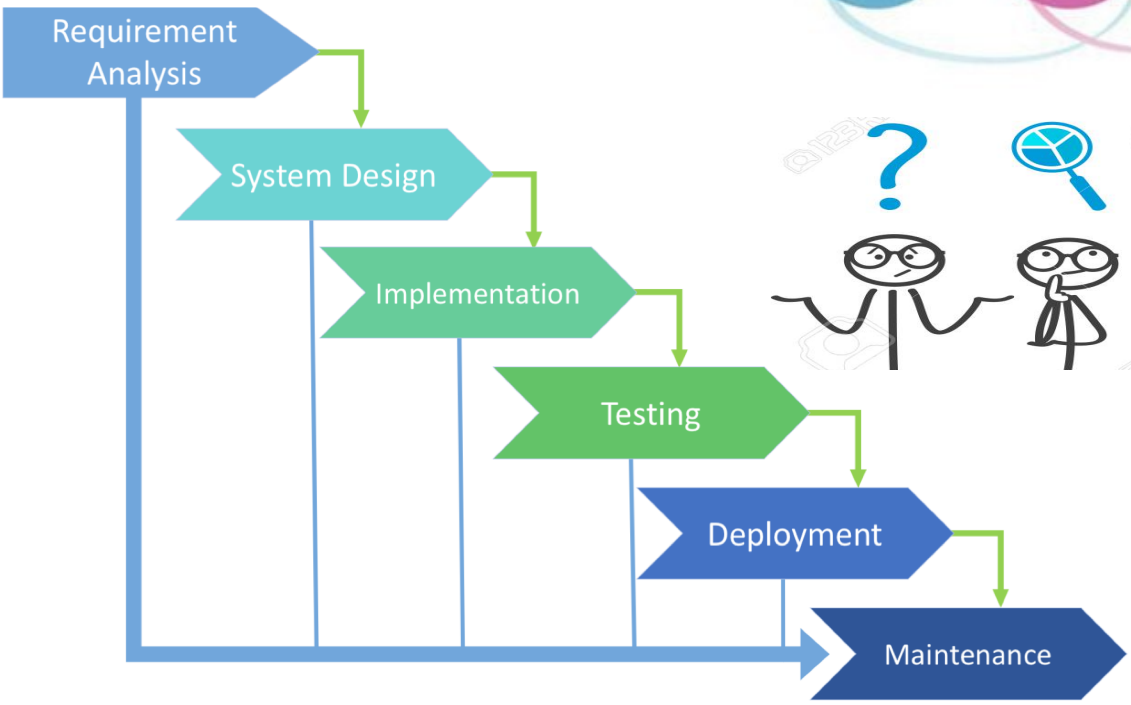
Edmodo

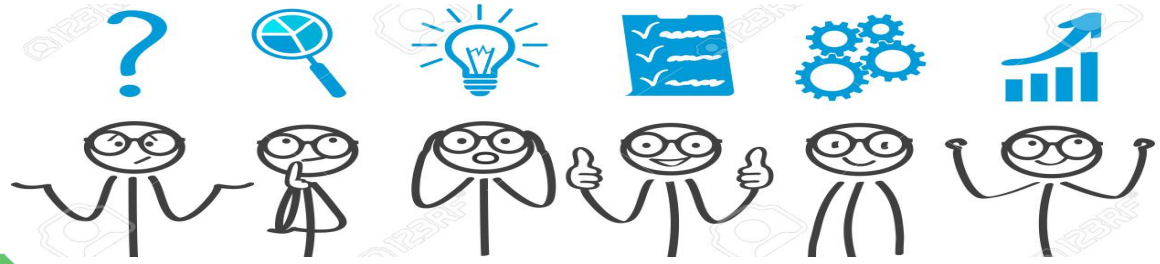
- Course slides
- Important announcements
- Code
  - Digital Logic Design
  - N4dqjv
  - https://edmo.do/j/euftnc

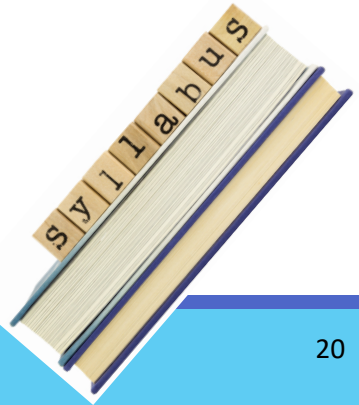
Course Syllabus at A Glance

- Digital Logic Circuit Design (DLCD)





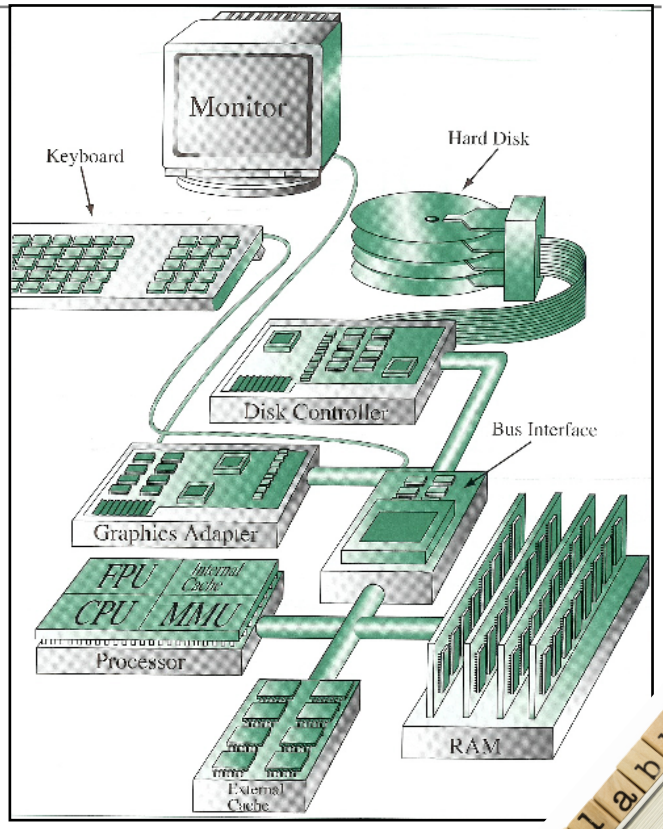


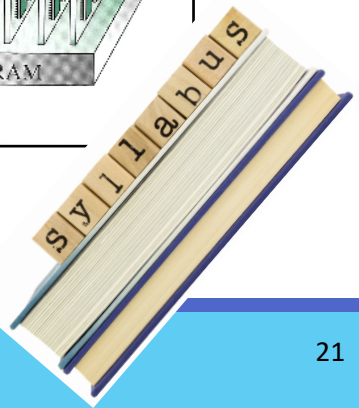


Course Syllabus In Detail

- **Digital computers and information**
  - Introduction
  - Concepts
  - Number system

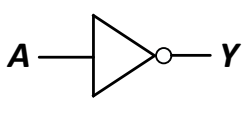
Base 10	Binary 2	Octal 8	Hex 16	BCD
08	1000	10	8	1000
15	1111	17	F	0001 0101



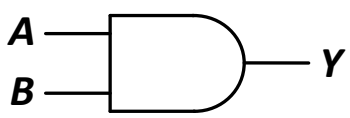


Course Syllabus in Detail (cont'd)

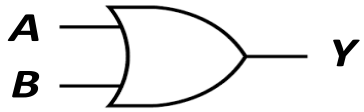
- **Design logic**
  - Boolean algebra
  - Switching function
  - Basic components



$(Y = \overline{A})$

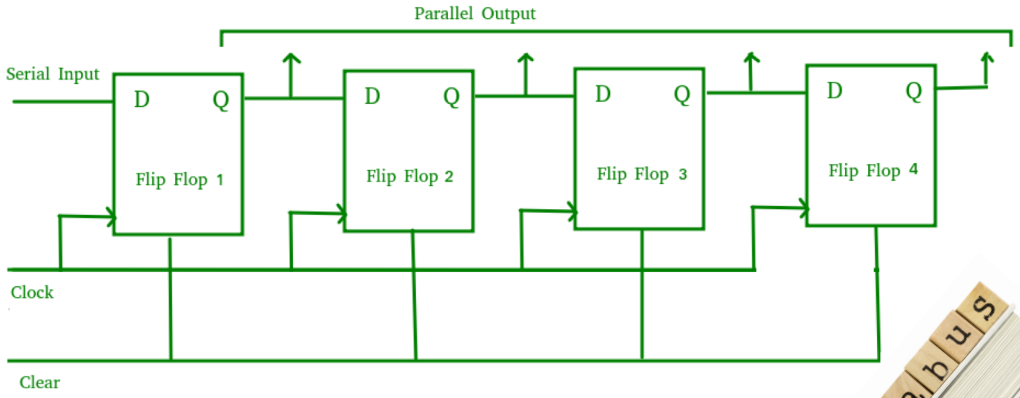


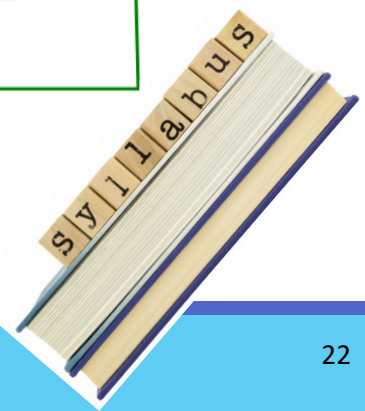
$(Y = A \cdot B)$



$(Y = A + B)$

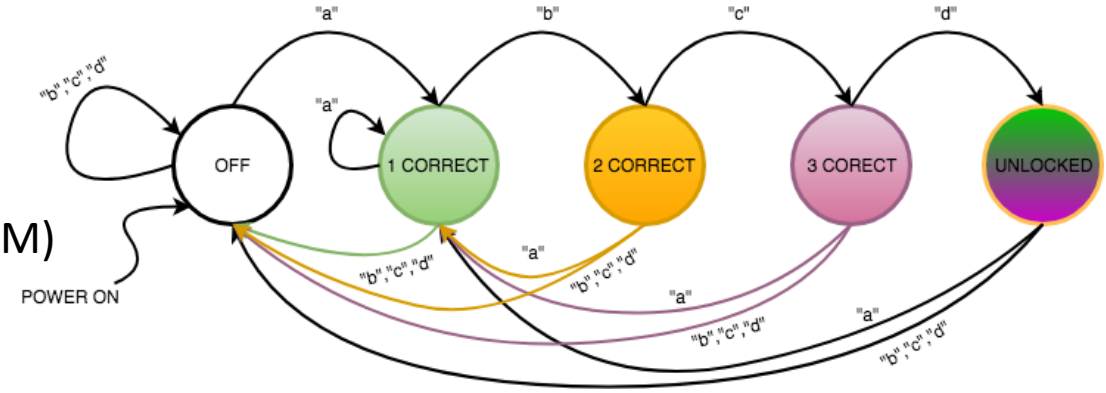
- **Design logic blocks**
  - Basic components
  - Combinational blocks
  - Storage components
  - Sequential blocks



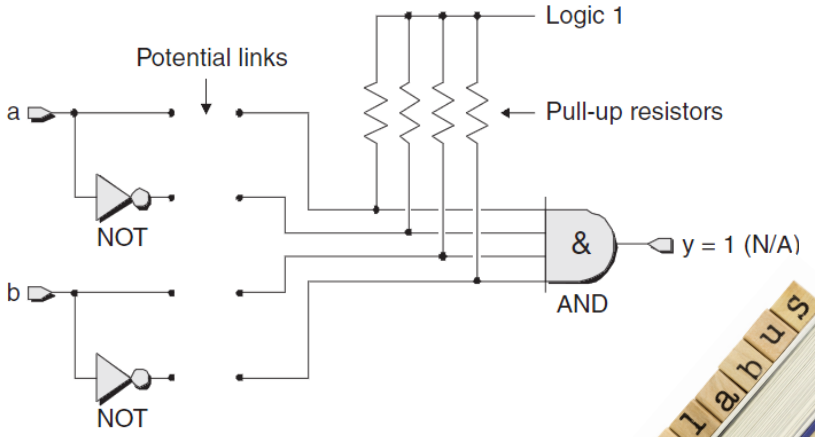


Course Syllabus in Detail (cont'd)

- **Design logic modeling**
  - **Model** the problem
  - Finite State Machine (FSM)
  - Algorithm State Machine (ASM)

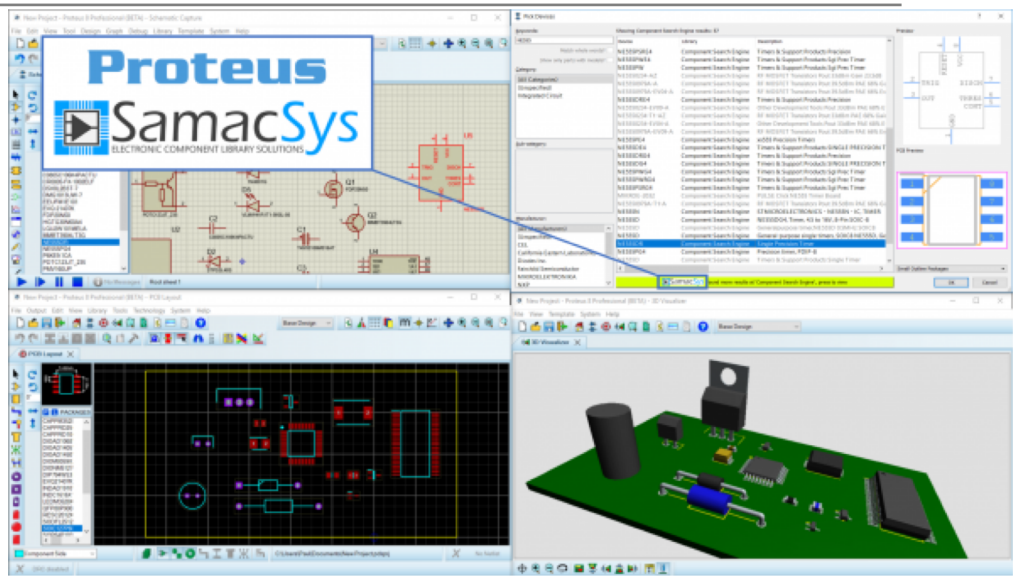


- **Design logic design**
  - Combinational design
  - Sequential design
  - Optimization
  - **Programmable** Logic Device (PLDs)



Design Tools

- **Design and simulation tools**
  - Proteus
  - Xilinx ISE tool set
  - Quartus



Quartus® Prime
Design Suite

Thank You